3A Ultra Low-Dropout CMOS Regulator

General Description

The AME8943 is positive CMOS linear regulator provided ultra low-dropout voltage (350mV @3A) and very low input range. It operates with a V_{IN} as low as 0.9V and V_{CTRL} voltage 2.7V with programmable output voltage as low as 0.8V. The AME8943 features ultra low dropout, ideal for applications where V_{OUT} is very close to V_{IN}. Additionally, It provides a power good signal to indicate if the voltage level of V_{OUT} reaches 90% of its rating value.

AME8943 is available in the SOP-8/PP and DFN-10B (3x3x0.75mm) packages.

Features

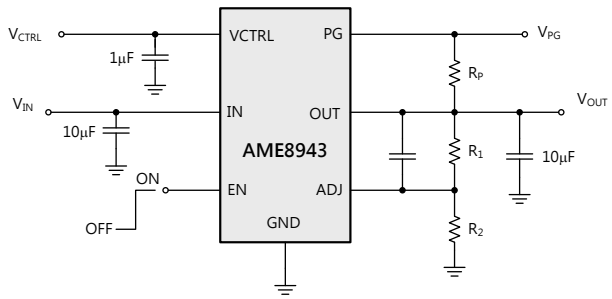
- Input Voltage Range: 0.9V to 5.5V
- VCTRL Range: 2.7V to 5.5V
- Output Voltage Range: 0.8V to 4V
- Low Dropout Voltage: 350mV @3A
- Output Noise: 57.6μVrms
- ±1.5% Output Accuracy
- Power-Good Output
- Built-In Soft-Start and Inrush Current Control
- OUT pin Pull Low Resistance when Disable
- RoHS, Halogen Free and TSCA Compliance

Application

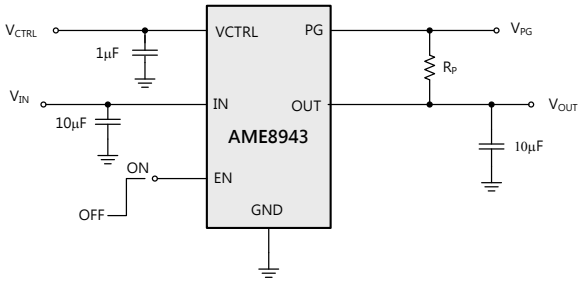
- Notebooks
- Tablet PCs
- Consumer Electronics
- Set-top Boxes
- Residential Gateways
- Telecom Systems
- Solid-State Drives (SSD)

Typical Application Schematic

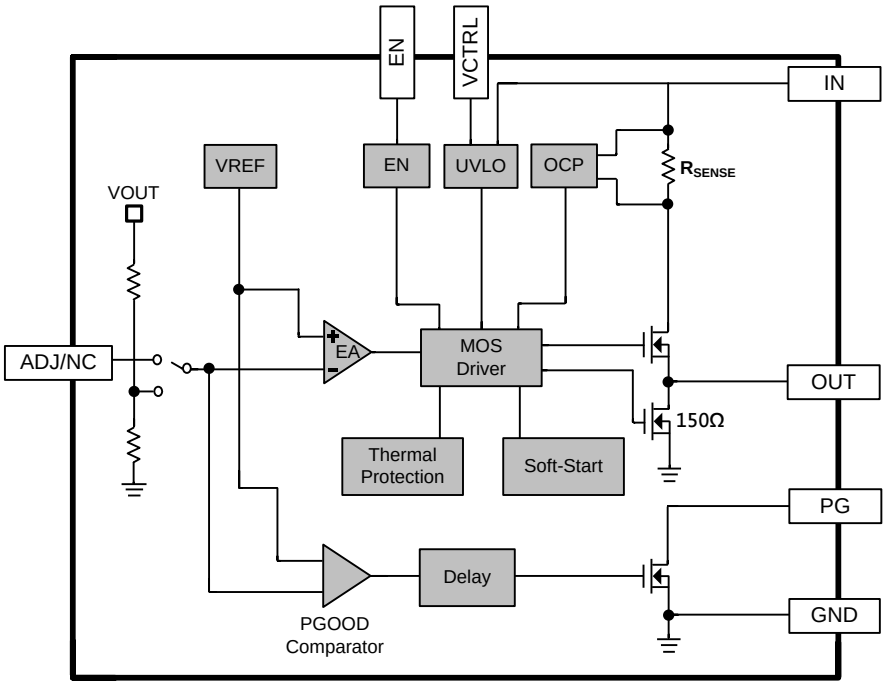
ADJ Version



Fixed Version

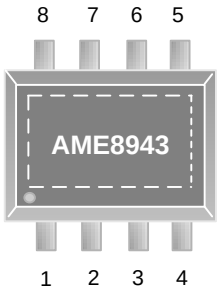


■ Function Block Diagram



■ Pin Configuration

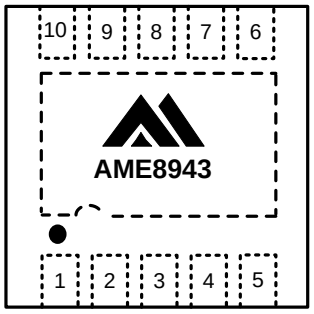
SOP-8/PP
Top View



AME8943x-AZAADJ

1. PG
2. EN
3. IN
4. VCTRL
5. NC
6. OUT
7. ADJ
8. GND

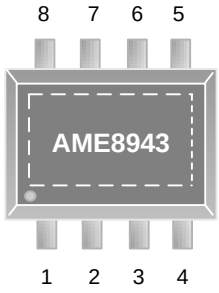
DFN-10B
(3x3x0.75mm)
Top View



AME8943x-AVBADJ

1. OUT
2. OUT
3. OUT
4. ADJ
5. PG
6. EN
7. IN
8. IN
9. IN
10. VCTRL

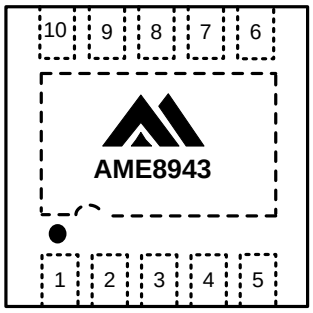
SOP-8/PP
Top View



AME8943x-BZAxxx

1. PG
2. EN
3. IN
4. VCTRL
5. NC
6. OUT
7. NC
8. GND

DFN-10B
(3x3x0.75mm)
Top View



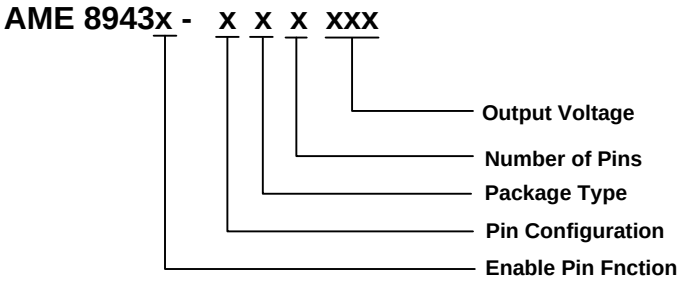
AME8943x-BVBxxx

1. OUT
2. OUT
3. OUT
4. NC
5. PG
6. EN
7. IN
8. IN
9. IN
10. VCTRL

■ Pin Description

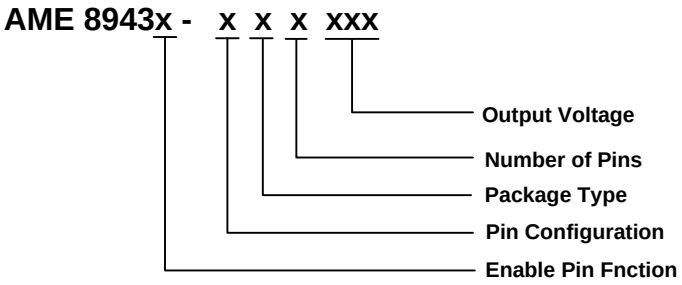
Pin Name	I/O	Pin Description	Pin Number			
			SOP-8/PP		DFN-10B	
			A	B	A	B
PG	O	Power Good Open Drain Output.	1	1	5	5
EN	I	Enable Input.	2	2	6	6
IN	I	Input Voltage.	3	3	7, 8, 9	7, 8, 9
VCTRL	I	Control Input Voltage.	4	4	10	10
NC	-	No Connection.	5	5,7	NA	4
OUT	O	Output Voltage.	6	6	1, 2, 3	1, 2, 3
ADJ	I	Set the output voltage by the external feedback resistors.	7	NA	4	NA
GND	-	Ground.	8	8	11	11

■ Ordering Information



Enable Pin Function	Pin Configuration	Package Type	Number of Pins	Output Voltage
A: Active High / Internal Pull High B: Active High / Internal Pull Low C: Active Low / Internal Pull High D: Active Low / Internal Pull Low	A (SOP-8/PP) 1. PG 2. EN 3. IN 4. VCTRL 5. NC 6. OUT 7. ADJ 8. GND A (DFN-10B) 1. OUT 2. OUT 3. OUT 4. ADJ 5. PG 6. EN 7. IN 8. IN 9. IN 10. VCTRL	V : DFN Z: SOP/PP	A: 8 B: 10	ADJ: Adjustable

■ Ordering Information (Contd.)



Enable Pin Function	Pin Configuration	Package Type	Number of Pins	Output Voltage
A: Active High / Internal Pull High B: Active High / Internal Pull Low C: Active Low / Internal Pull High D: Active Low / Internal Pull Low	B (SOP-8/PP) 1. PG 2. EN 3. IN 4. VCTRL 5. NC 6. OUT 7. NC 8. GND B (DFN-10B) 1. OUT 2. OUT 3. OUT 4. NC 5. PG 6. EN 7. IN 8. IN 9. IN 10. VCTRL	V : DFN Z: SOP/PP	A: 8 B: 10	250: 2.5V

■ Absolute Maximum Ratings

Parameter		Value	Unit
Input Voltage		-0.3 to 6	V
Enable Voltage		-0.3 to 6	
Output Voltage		-0.3 to 6	
Control Input Voltage		-0.3 to 6	
Power Good Pin		-0.3 to 6	
ESD Rating	HBM	±2000	
	MM	±200	
	CDM	±1000	

■ Recommended Operation Conditions

Parameter	Symbol	Rating	Unit
Input Voltage	V_{IN}	0.9 to 5.5	V
Control Input Voltage	V_{CTRL}	2.7 to 5.5	V
Ambient Temperature Range	T_A	-40 to +85	°C
Junction Temperature Range	T_J	-40 to +125	
Storage Temperature Range	T_{STG}	-55 to +150	

■ Thermal Information

Parameter	Package	Die Attach	Symbol	Maximum	Unit
Thermal Resistance* (Junction to Case)	SOP-8/PP	Conductive Epoxy	θ_{JC}	19	°C / W
	DFN-10B			8.5	
Thermal Resistance (Junction to Ambient)	SOP-8/PP		θ_{JA}	84	
	DFN-10B			65	
Power Dissipation	SOP-8/PP		P_D	1450	mW
	DFN-10B			1540	
Lead Temperature (Soldering 10 Sec)**				260	°C

* Measure θ_{JC} on backside center of Exposed Pad.

** MIL-STD-202G210F

■ Electrical Specifications

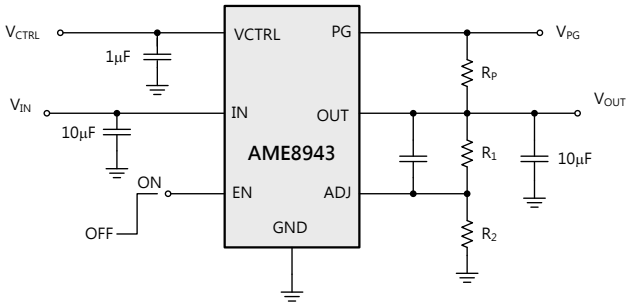
V_{IN} = V_{OUT} + 0.5V, V_{CTRL} = V_{EN} = 5V, I_{OUT} = 1mA, C_{IN} = C_{OUT} = 10µF, C_{CTRL} = 1µF, unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Power Input Voltage Range	V_{IN}		0.9		V_{CTRL}-1.5	V
V_{IN} POR Threshold	V_{IN-POR}	V_{IN} Rising		0.79		V
V_{IN} POR Hysteresis	ΔV_{IN-POR}			0.1		
V_{CTRL} POR Threshold	$V_{CTRL-POR}$	V_{CNTL} Rising		2.3		
V_{CTRL} POR Hysteresis	$\Delta V_{CTRL-POR}$			0.2		
Quiescent Current (V_{CTRL})	I_{Q_CTRL}	EN On, No Load		400		µA
Quiescent Current (V_{IN})	I_{Q_IN}	EN On, No Load		12	40	
Shutdown Current (V_{IN})	I_{SHDN_IN}	V_{EN} = 0V			0.5	
Shutdown Current (V_{CTRL})	I_{SHDN_CTRL}	V_{EN} = 0V			0.5	
Reference Voltage	V_{ADJ}		0.788	0.8	0.812	V
Output Voltage Accuracy	$V_{OUT-ACC}$	Fix Output	-1.5		1.5	%
Line Regulation	REG_{LINE}	V_{CNTL} = 2.7V to 5.5V, V_{IN} = V_{OUT} + 0.5V to 5.5V, I_{OUT} = 1mA		0.2	0.5	
Load Regulation	REG_{LOAD}	I_{OUT} = 1mA to 3A		0.3	0.9	
Dropout Voltage	V_{DROP}	I_{OUT} = 3A		350	450	mV
		I_{OUT} = 2A		180	250	
Current Limit	I_{LIM}		3.2	4.4	5.8	A
Short Circuit Current	I_{SC}	V_{OUT} < 0.25V	0.5	1	1.7	
V_{OUT} Pull Low Resistance	R_{DIS}	V_{CNTL} = 5.5V		100		Ω
EN High Level	$V_{EN(HI)}$		0.9			V
EN Low Level	$V_{EN(LO)}$				0.4	
EN Pin Bias Current	I_{EN}	V_{EN} = 5V		0.15	1	µA
PG Threshold Voltage		V_{OUT} Rising		90		%
PG Hysteresis		V_{OUT} Falling		10		%
PG Delay Time				1.1		ms
PG Low Voltage		PG sinks 10mA		0.1	0.2	V
V_{OUT} Noise		10Hz to 100KHz		57.6		μV_{rms}
Soft-Start Time	T_{SS}		0.4	1	2	ms
Over Temperature Shutdown	T_{SHDN}			160		°C
Over Temperature Hysteresis	$T_{SHDN-HYS}$			30		°C

■ Application Information

Adjustable Mode Operation

The output voltage of the AME8943 is adjustable from 0.8V to V_{IN} by external voltage divider resisters as shown as below.



R1 and R2 should be more than 10kΩ to reduce the power loss. The output voltage can be calculated by the following equation:

$$V_{OUT} = 0.8 \ X \ \frac{(R_1+R_2)}{R_2}$$

Input Capacitor

Bypass capacitor is required to improve AC performance and recommended from input to ground. A 10µF or greater located as close as possible to AME8943 is recommended.

Output Capacitor

It was required to fulfill both requirements for minimum amount of capacitance and ESR in all LDOs application by output capacitor. The ESR of output capacitor relates to stability. The AME8943 specifically work with low ESR ceramic output capacitor in space-saving and performance consideration. At least 10µF ceramic capacitor was placed at AME8943 output to ensure stability.

In addition, the AME8943 still works well with output capacitor of other types due to the wide stable ESR range. Larger output capacitance is able to reduce noise and enhance load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the V_{OUT} pin and returned to a clean analog ground.

Enable

Operation mode: EN pin is in the logic high condition.
Shutdown mode: EN pin is in the logic low condition. During this condition, the pass transistor, error amplifier, and band gap are turned off, reducing the supply current to 0.15µA typical.

If the EN pin is floating, please pay attention to AME8943 internal initial logic level. Internally EN pin function pulls low level. So the regulator will be turned off.

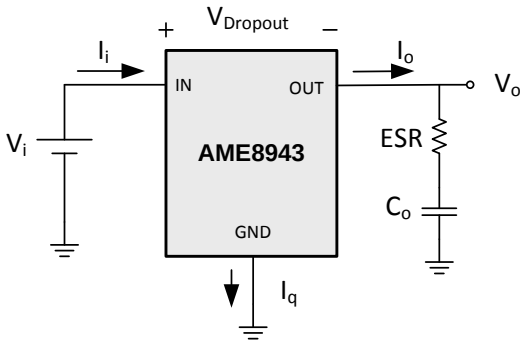
Power Good

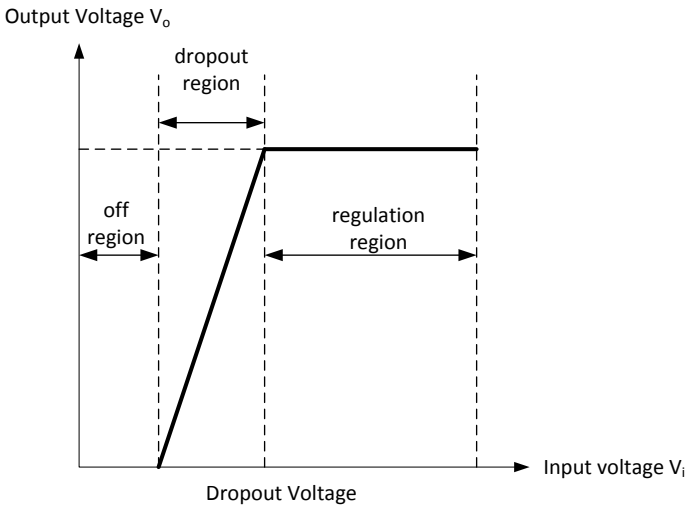
The power good function is an open-drain output and need a 100kΩ pull-up resistor. Be placed at OUT pin to get output voltage. The PG pin will output high immediately after the output voltage reaches 90% of normal output voltage.

■ Application Information (Contd.)

Dropout Voltage

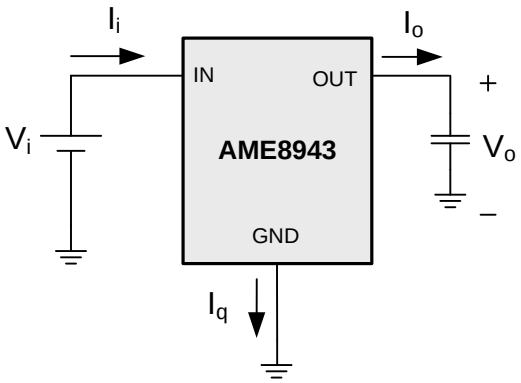
Dropout voltage is a differential voltage between input and output at which the IC ceases to regulate against further reductions in input voltage; this timing occurs when the input voltage approaches the output voltage. In the dropout region, the pass element act as a resistor and dropout is expressed in terms of its on-resistance(Ron).





Quiescent Current

Quiescent, or ground current, is the difference between input and output currents. Low quiescent current is necessary to maximize the current efficiency.

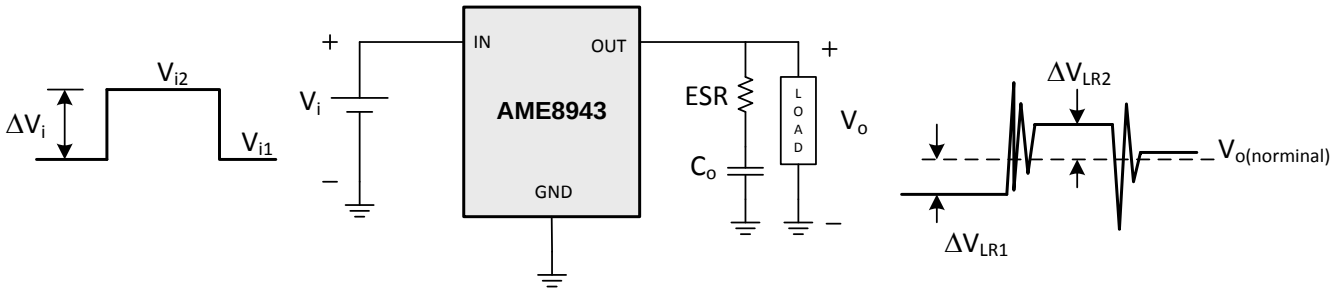


Quiescent Current $I_q = I_i - I_o$

■ Application Information (Contd.)

Line Regulation

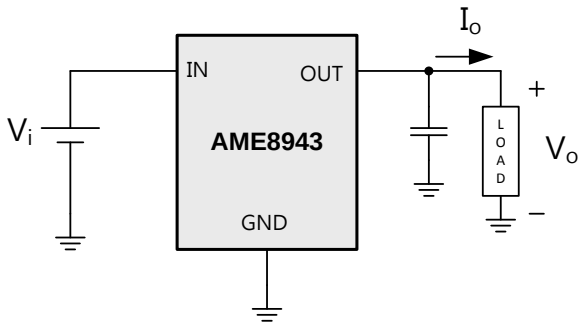
Line regulation is a measure of the IC's ability to maintain the nominal output voltage with varying input voltage.



$$\text{Line Regulation} = \frac{\Delta V_O}{\Delta V_i}$$

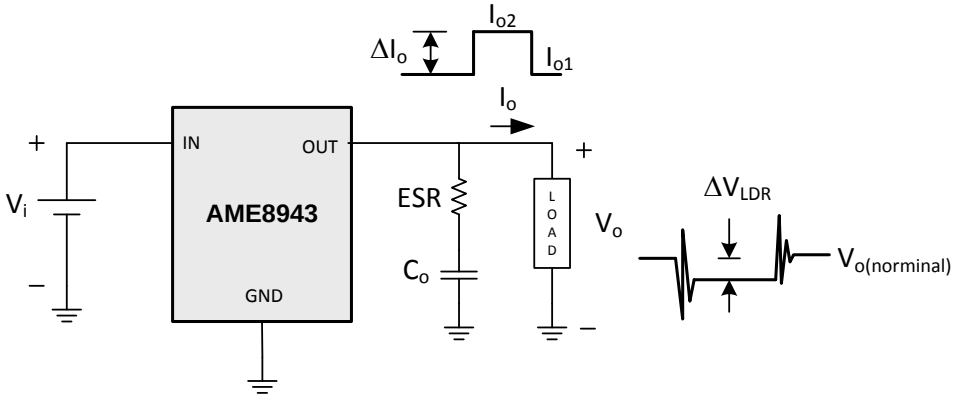
Load Regulation

Load regulation is a measure of the IC's ability to maintain the specified output voltage under varying load conditions.



$$\text{Load Regulation} = \frac{\Delta V_O}{\Delta I_O}$$

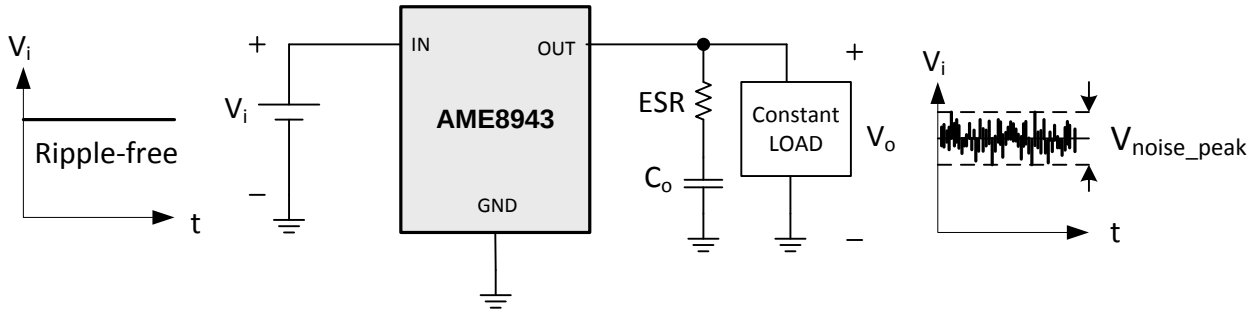
The worst case of the output voltage variations occurs as the load current transitions from zero to its maximum rated value or vice versa, which is illustrated in following figure. The load regulation is determined by the ΔV_{LDR} since load regulation is a steady-state parameter like the line regulation.



■ Application Information (Contd.)

Output Noise Voltage

It is the RMS output noise voltage over a given range of frequencies (10Hz to 100KHz) under the situations of a constant output current and a ripple-free input voltage. The noise generated only by IC becomes the output noise voltage. Most output noise is induced by the internal voltage reference of LDO.



Efficiency

The efficiency is determined by the quiescent current and input/output voltages as follows.

$$\text{Efficiency} = \frac{I_O V_O}{(I_O+I_q)V_i} \times 100$$

To increase efficiency, drop out voltage and quiescent current must be minimized. In addition, the voltage difference between input and output must be minimized, since the power dissipation of LDO accounts for the efficiency. (Power Dissipation = (Vi – Vo)Io). The input/output voltage difference is an intrinsic factor in determining the efficiency, regardless of the load condition

Power Dissipation

Power dissipation caused by voltage drop across the LDO and by the output current flowing through the device needs to be dissipated out from the chip. The maximum power dissipation is dependent on the PCB layout, number of used Cu layers, Cu layers thickness and the ambient temperature.

The maximum power dissipation can be computed by following equation:

$$P_{D(MAX)} = \frac{T_J - T_A}{\theta_{JA}}$$

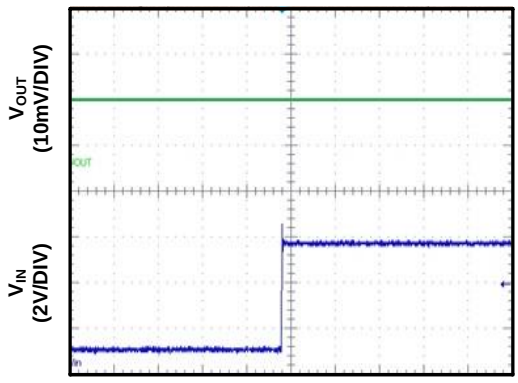
Where ($T_J - T_A$) is the temperature difference between the junction and ambient temperatures and θ_{JA} is the thermal resistance (dependent on the PCB as mentioned above).

$$P_D = V_{IN} I_{GND} + (V_{IN} - V_{OUT}) I_{OUT}$$

Where I_{GND} is the LDO's ground current which dependent on the output load current. Connecting the exposed pad and NC pin to a large ground planes helps to dissipate the heat from the chip.

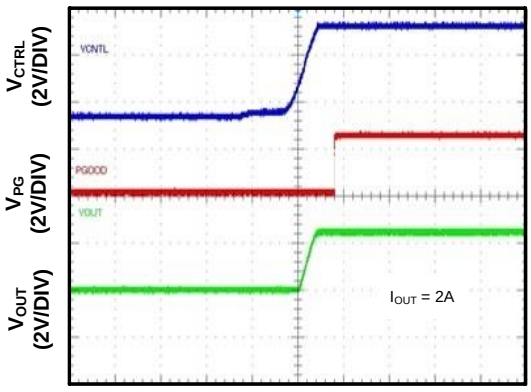
■ Characterization Curve

V_{IN} Line Transient Response



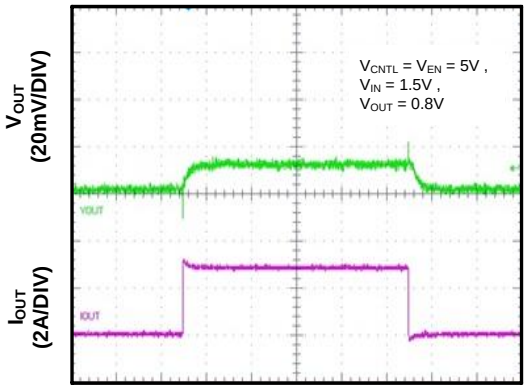
Time (20ms/DIV)

Star Up from V_{CTRL}



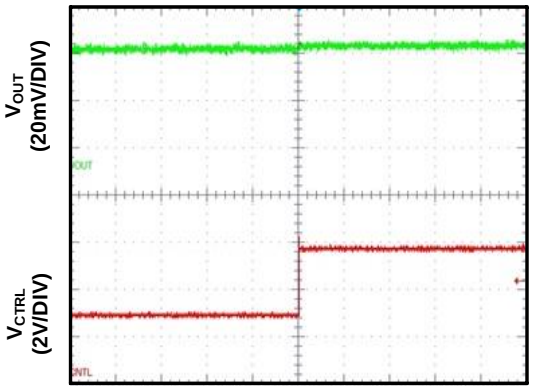
Time (2ms/DIV)

Load Regulation



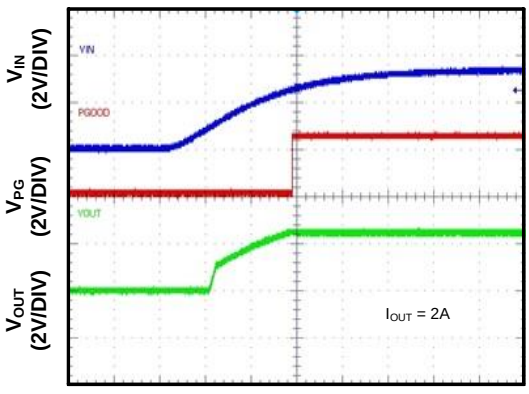
Time (1ms/DIV)

V_{CTRL} Line Transient Response



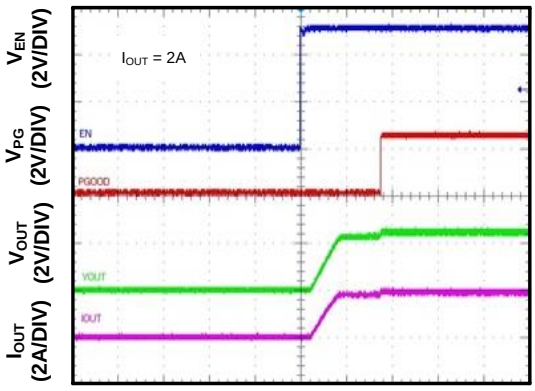
Time (20ms/DIV)

Start Up from V_{IN}



Time (2ms/DIV)

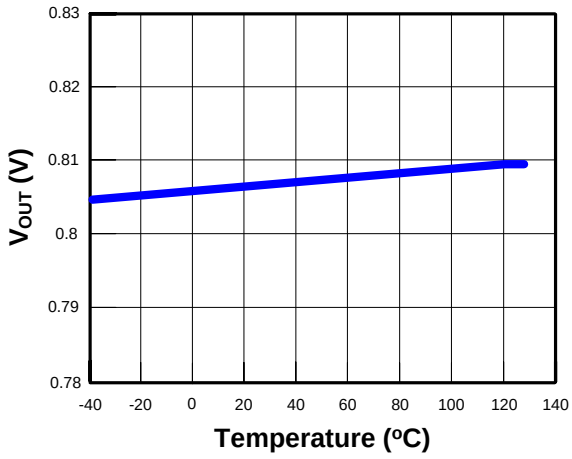
Start Up from Enable



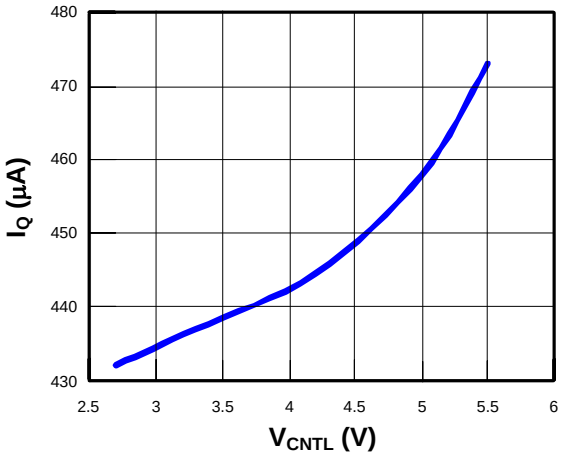
Time (1ms/DIV)

■ Characterization Curve (Contd.)

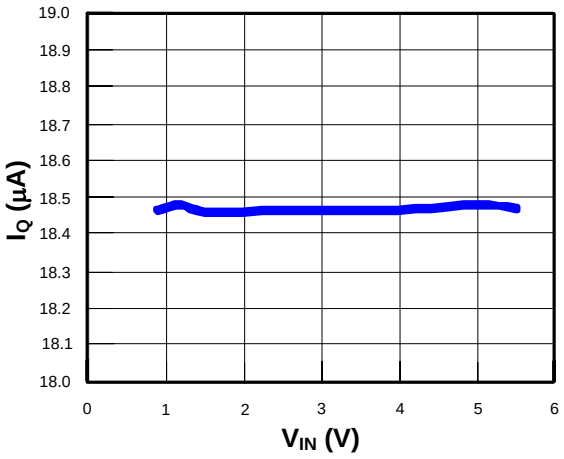
V_{OUT} vs. Temperature



V_{CNTL} vs. I_Q

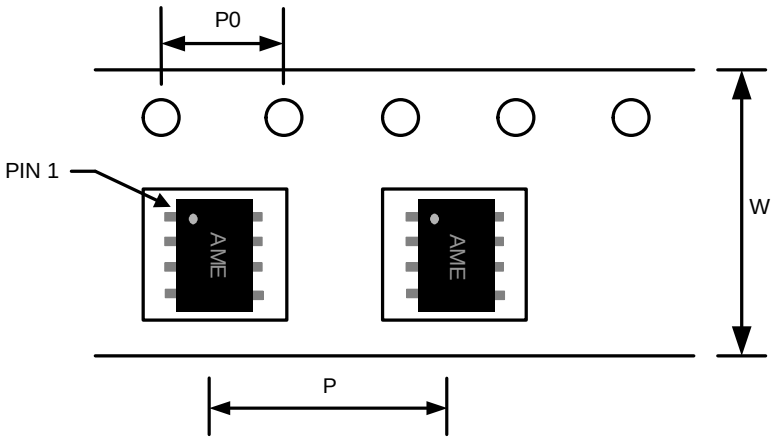


V_{IN} vs. I_Q



■ Tape and Reel Dimension

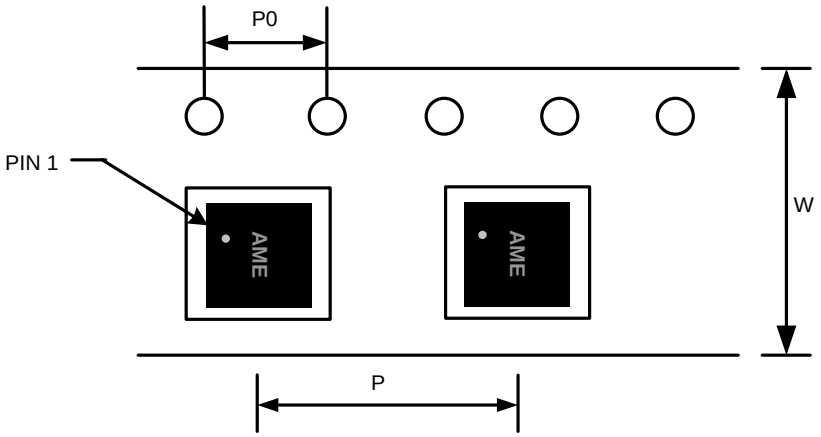
SOP-8/PP



Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Pitch (P0)	Part Per Full Reel	Reel Size
SOP-8/PP	12.0±0.1 mm	8.0±0.1 mm	4.0±0.1 mm	2500pcs	330±1 mm

DFN-10B
(3x3x0.75mm)



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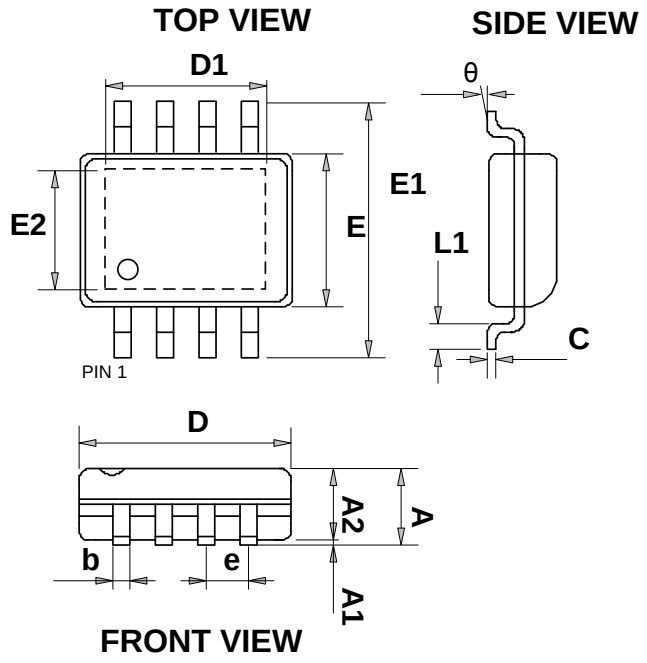
Package	Carrier Width (W)	Pitch (P)	Pitch (P0)	Part Per Full Reel	Reel Size
DFN-10B	12.0±0.1 mm	8.0±0.1 mm	4.0±0.1 mm	3000pcs	330±1 mm

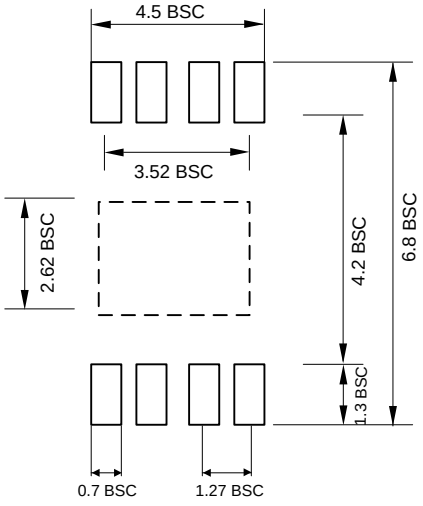
■ Package Dimension

SOP-8/PP



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.000	0.150	0.000	0.006
A2	1.350	1.600	0.053	0.063
C	0.100	0.250	0.004	0.010
E	3.750	4.150	0.148	0.163
E1	5.700	6.300	0.224	0.248
L1	0.300	1.270	0.012	0.050
b	0.310	0.510	0.012	0.020
D	4.720	5.120	0.186	0.202
e	1.270 BSC		0.050 BSC	
θ	0^o	8^o	0^o	8^o
E2	2.150	2.513	0.085	0.099
D1	2.150	3.402	0.085	0.134

■ Lead Pattern

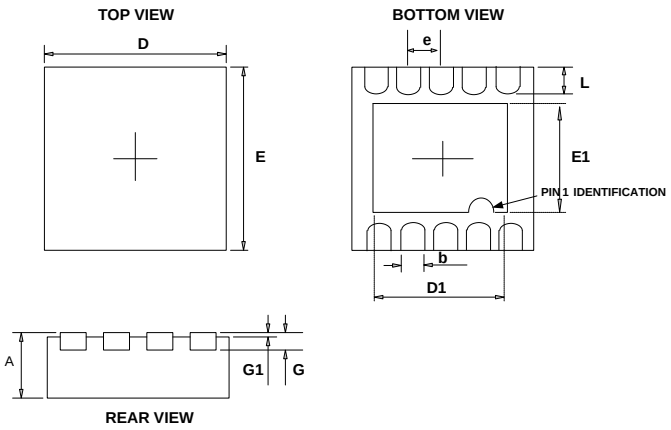


Note:

1. Lead pattern unit description:
   BSC: Basic. Represents theoretical exact dimension or dimension target.
2. Dimensions in Millimeters.
3. General tolerance ±0.05mm unless otherwise specified.

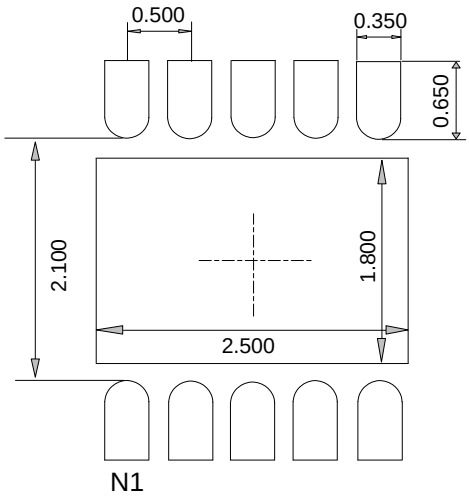
■ Package Dimension (Contd.)

DFN-10B (3x3x0.75mm)



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
e	0.450	0.550	0.018	0.022
D1	2.300	2.500	0.091	0.098
E1	1.600	1.800	0.063	0.071
b	0.180	0.300	0.007	0.012
L	0.300	0.500	0.012	0.020
G	0.153	0.253	0.006	0.010
G1	0.000	0.050	0.000	0.002

■ Lead Pattern



Note:

4. Lead pattern unit description:
   BSC: Basic. Represents theoretical exact dimension or dimension target.
5. Dimensions in Millimeters.
6. General tolerance ±0.05mm unless otherwise specified.

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