Low Quiescent Current, Adjustable Voltage Monitoring, Adjustable Reset Delay Supervisory

■ General Description

The AME8505 series of microprocessor supervisory circuits monitors system voltages from 0.405V to 5V, asserting an open-drain $\overline{\text{RESET}}$ signal when the SENSE voltage drops below a preset threshold or when the manual reset ($\overline{\text{MR}}$) pin drops to a logic low. The $\overline{\text{RESET}}$ output remains low for the user-adjustable delay time after the SENSE voltage and $\overline{\text{MR}}$ return above the respective thresholds.

The AME8505 device adopts a precision reference to achieve 0.5% threshold accuracy for $V_{IT} \leq 3.3V$. The reset delay time can be set to 20ms by disconnecting the C_T pin, 300ms by connecting the C_T pin to V_{DD} using a resistor or can be user-adjusted between 1.25ms and 10s by connecting the C_T pin to an external capacitor. The AME8505 device has a very low typical quiescent current of 1.7μA, so it is well-suited to battery-powered applications.

■ Features

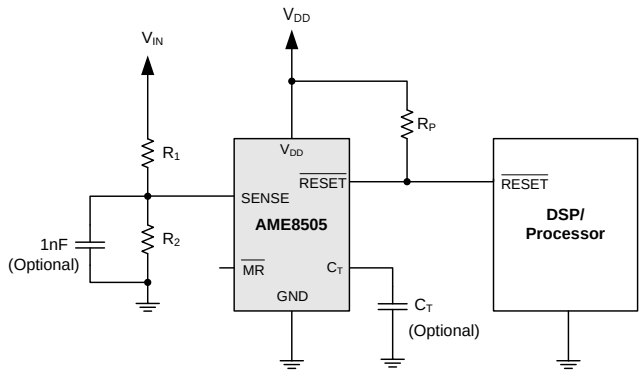
- Power-On Reset Generator with Adjustable Delay Time: 1.25ms to 10s
- Very Low Quiescent Current: 1.7μA
- High Threshold Accuracy: 0.5% Typical
- Fixed Threshold Voltages for Standard Voltage from 0.9V to 5V
- Adjustable Voltage Down to 0.405V are Available
- Provide $\overline{\text{MR}}$ Input
- Open-Drain $\overline{\text{RESET}}$ Output
- Temperature Range: –40°C to +125°C
- SOT-26 and DFN-6D(2x2x0.75mm) Packages

■ Application

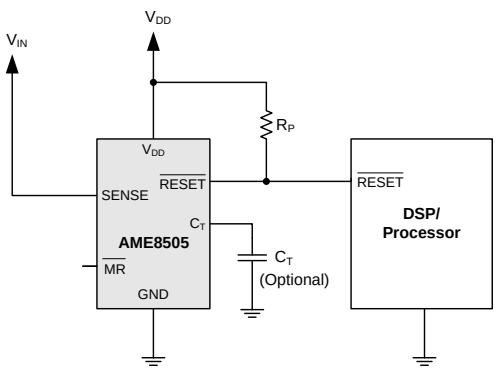
- DSP or Microcontroller Applications
- Notebook and Desktop Computers
- PDAs and Hand-Held Products
- Portable and Battery-Powered Products
- FPGA and ASIC Applications

■ Typical Application Schematic

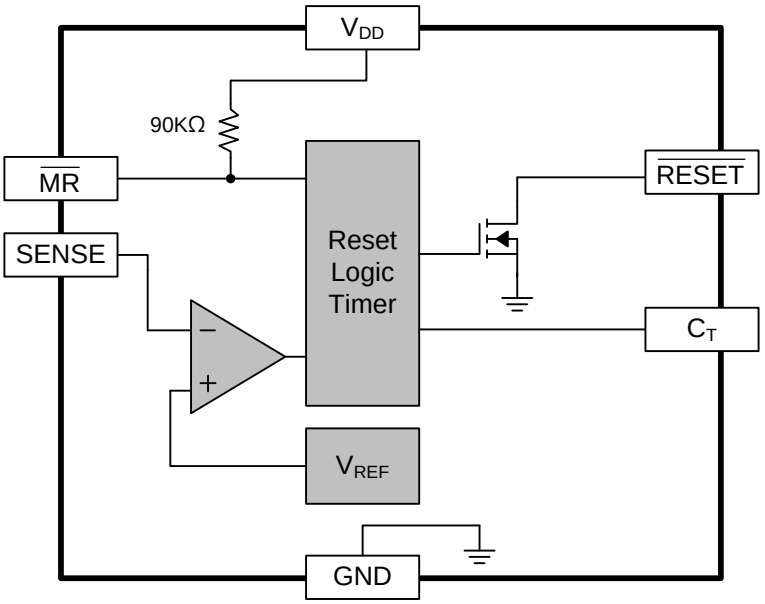
ADJ Version



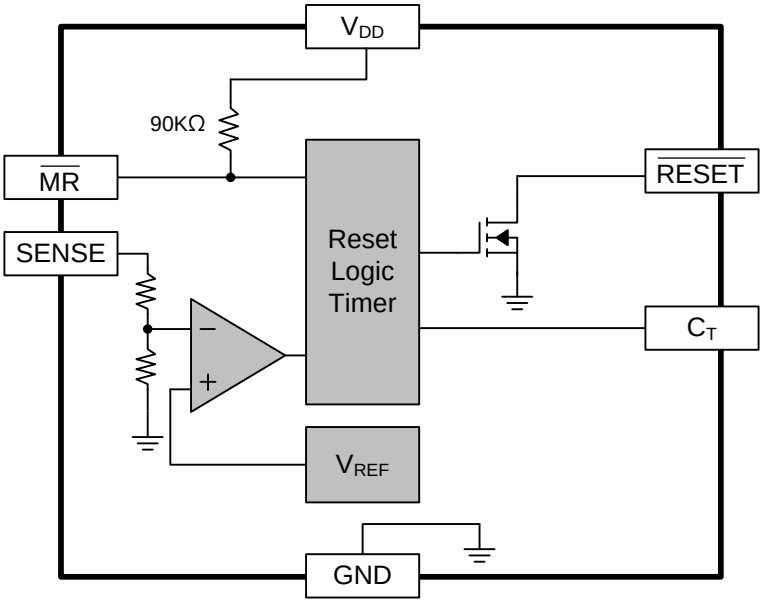
Fixed Version



■ Block Diagram



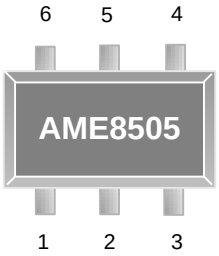
Adjustable Voltage Version



Fixed Voltage Version

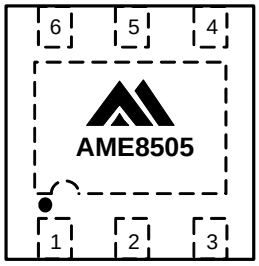
■ Pin Configuration

SOT-26
Top View



AME8505-AEYxxx
1. $\overline{\text{RESET}}$
2. GND
3. $\overline{\text{MR}}$
4. C_T
5. SENSE
6. V_{DD}

DFN-6D
(2x2x0.75mm)
Top View

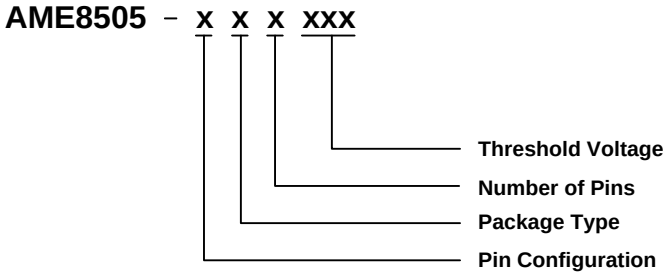


AME8505-AVYxxx
1. V_{DD}
2. SENSE
3. C_T
4. $\overline{\text{MR}}$
5. GND
6. $\overline{\text{RESET}}$

■ Pin Description

Pin No.		Pin Name	I/O	Pin Description
SOT-26	DFN-6D (2x2x0.75mm)			
1	6	$\overline{\text{RESET}}$	O	$\overline{\text{RESET}}$ is an open-drain output that is driven to a low-impedance state when $\overline{\text{RESET}}$ is asserted (either the SENSE input is lower than the threshold voltage (V_{IT}) or the $\overline{\text{MR}}$ pin is set to a logic low). $\overline{\text{RESET}}$ will keep low (asserted) for the reset period after both SENSE is above V_{IT} and $\overline{\text{MR}}$ is set to a logic high. A pull-up resistor from 10kΩ to 1MΩ should be used on this pin, and allows the reset pin to attain voltages higher than V_{DD}.
2	5	GND	NA	Ground pin. This pin should be connected to PCB ground reference.
3	4	$\overline{\text{MR}}$	I	Manual Reset Input pin. $\overline{\text{MR}}$ low asserts $\overline{\text{RESET}}$. $\overline{\text{MR}}$ is internally tied to V_{DD} by 90kΩ a pull-up Resistor.
4	3	C_T	I	Reset Period Programming pin. Connecting this pin to V_{DD} through a 40kΩ to 200kΩ resistor or leaving it open results in fixed reset delay times. Connecting this pin to a ground referenced capacitor (≥100pF) gives a user programmable reset delay time.
5	2	SENSE	I	This pin is connected to the voltage to be monitored. If the voltage at this terminal drops below the threshold voltage V_{IT}, then $\overline{\text{RESET}}$ is asserted. SENSE does not necessary monitor V_{DD}, it can monitor any voltage lower than V_{DD}.
6	1	V_{DD}	I	Supply Voltage. A 0.1μF ceramic capacitor placed close to this pin is helpful for transient and parasitic.
NA	Pad	Thermal Pad	NA	Thermal Pad. Connect to ground plane to enhance thermal performance of package.

■ Ordering Information



Pin Configuration		Package Type	Number of Pins	Threshold Voltage
A (SOT-26)	1. $\overline{\text{RESET}}$ 2. GND 3. $\overline{\text{MR}}$ 4. C_T 5. SENSE 6. V_{DD}	E: SOT-2X V: DFN	Y: 6	ADJ: 0.405V 084: 0.84V 112: 1.12V 167: 1.67V 279: 2.79V 307: 3.07V 465: 4.65V
A (DFN-6D)	1. V_{DD} 2. SENSE 3. C_T 4. $\overline{\text{MR}}$ 5. GND 6. $\overline{\text{RESET}}$			

■ Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage	V_{DD}	-0.3 to 7	V
	V_{CT}	-0.3 to V_{DD} + 0.3	
	$V_{\overline{RESET}}$, $V_{\overline{MR}}$, V_{SENSE}	-0.3 to 7	
Current	$\overline{RESET}$	-5 to 5	mA
ESD Classification	HBM	±2000	V
	MM	±200	V
	CDM	±1000	V

■ Recommended Operation Conditions

Parameter	Symbol	Rating	Unit
Input Supply Voltage	V_{DD}	1.7 to 6.5	V
C_T Pin Voltage	V_{CT}	0 to V_{DD}	
Sense Pin Voltage	V_{SENSE}	0 to 6.5	
$\overline{MR}$ Pin Voltage	$V_{\overline{MR}}$	0 to 6.5	
$\overline{RESET}$ Pin Voltage	$V_{\overline{RESET}}$	0 to 6.5	
$\overline{RESET}$ Pin Current	$I_{\overline{RESET}}$	0.0003 to 5	mA
Junction Temperature Range	T_J	-40 to +125	°C
Ambient Temperature Range	T_A	-40 to +85	
Storage Temperature Range	T_{STG}	-65 to +150	

■ Thermal Information

Parameter	Package	Die Attach	Symbol	Maximum	Unit
Thermal Resistance* (Junction to Case)	SOT-26	Conductive Epoxy	θ_{JC}	81	°C / W
	DFN-6D			16	
Thermal Resistance (Junction to Ambient)	SOT-26	Conductive Epoxy	θ_{JA}	260	°C / W
	DFN-6D			66	
Internal Power Dissipation	SOT-26	Conductive Epoxy	P_D	400	mW
	DFN-6D			1515	
Lead Temperature (soldering 10 sec)**				260	°C

* Measure θ_{jc} on top of package.

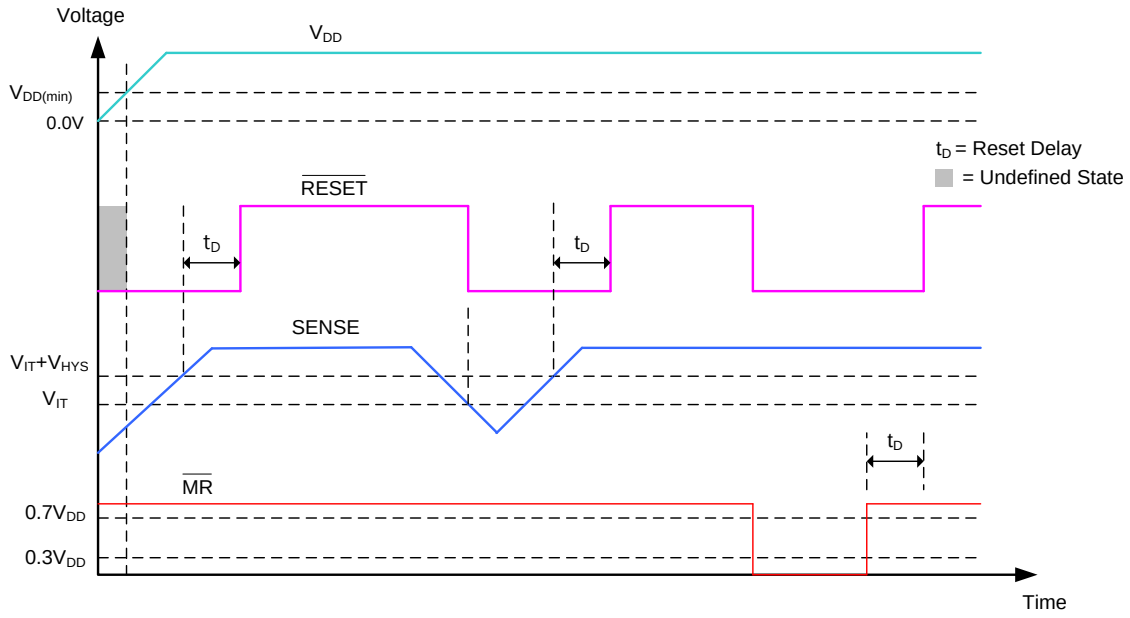
** MIL-STD-202G 210F

■ Electrical Specifications

$1.7V \leqq V_{DD} \leqq 6.5V$, $R_{LRESET} = 100k\Omega$, $C_{LRESET} = 50pF$, $T_A = 25^oC$, unless otherwise specified

Parameter		Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage Range		V_{DD}		1.7		6.5	V
Supply Current		I_{DD}	V_{DD} = 3V, $\overline{RESET}$ not asserted $\overline{MR}$, $\overline{RESET}$, C_T Open		1.4		μA
			V_{DD} = 6.5V, $\overline{RESET}$ not asserted $\overline{MR}$, $\overline{RESET}$, C_T Open		1.7		
Low-Level Output Voltage		V_{OL}	$1.3V \leqq V_{DD} \leqq 1.8V$, I_{OL} = 0.4mA			0.3	V
			$1.8V \leqq V_{DD} \leqq 6.5V$, I_{OL} = 1mA			0.4	
Power-Up Output Voltage		V_{POR}	$V_{OL(MAX)}$ = 0.2V, $I_{\overline{RESET}}$ = 15μA			0.8	V
Negative-going Input Threshold Accuracy		V_{IT}		-2		2	%
Hysteresis On V_{IT} PIN	ADJ Version	V_{HYS}			1.5	3	$\%V_{IT}$
	Fixed Version				1	2.5	
$\overline{MR}$ Internal Pull-Up Resistance		$R_{\overline{MR}}$		70	90		kΩ
Input Current at SENSE pin	ADJ Version	I_{SENSE}	$V_{SENSE} = V_{IT}$	-25		25	nA
	Fixed Version		V_{SENSE} = 6.5V		1.7		μA
$\overline{RESET}$ Leakage Current		I_{OH}	$V_{\overline{RESET}}$ = 6.5V, $\overline{RESET}$ not asserted			300	nA
Input Capacitance, any pin	C_T pin	C_{IN}	V_{IN} = 0V to V_{DD}		5		pF
	Other pins		V_{IN} = 0V to 6.5V		5		
$\overline{MR}$ Input Logic Low		V_{IL}		0		$0.3*V_{DD}$	V
$\overline{MR}$ Input Logic High		V_{IH}		$0.7*V_{DD}$			V
Input Pulse Width to $\overline{RESET}$	SENSE	t_W	V_{IH} = 1.05 V_{IT}, V_{IL} = 0.95 V_{IT}		20		μS
	$\overline{MR}$		V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}		0.001		
$\overline{RESET}$ Delay Time	C_T = Open	t_d		12	20	28	mS
	$C_T = V_{DD}$			180	300	420	mS
	C_T = 100pF			0.75	1.25	1.75	mS
	C_T = 180nF			0.7	1.2	1.7	S
Propagation Delay	$\overline{MR}$ to $\overline{RESET}$		V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}		150		nS
High to Low Level $\overline{RESET}$ Delay	SENSE to $\overline{RESET}$		V_{IH} = 1.05 V_{IT}, V_{IL} = 0.95 V_{IT}		20		μS

■ Timing Diagram



$\overline{MR}$	SENSE > V_{IT}	$\overline{RESET}$
L	0	L
L	1	L
H	0	L
H	1	H

Table1. Truth Table

Normal Operation (V_{DD} > $V_{DD(min)}$)

When V_{DD} is greater than $V_{DD(min)}$, the $\overline{RESET}$ signal is determined by the voltage on the SENSE pin and the logic state of $\overline{MR}$.

$\overline{MR}$ high: When the voltage on V_{DD} is greater than 1.7V for a time of the selected t_D, the $\overline{RESET}$ signal corresponds to the voltage on SENSE relative to V_{IT}.

$\overline{MR}$ low: in this mode, $\overline{RESET}$ is held low regardless of the value of the SENSE pin.

Above Power-On Reset but Less Than $V_{DD(min)}$ (V_{POR} < V_{DD} < $V_{DD(min)}$)

When the voltage on V_{DD} is less than the device $V_{DD(min)}$ voltage, and greater than the power-on reset voltage (V_{POR}), the $\overline{RESET}$ signal is asserted and low impedance, respectively, regardless of the voltage on the SENSE pin.

Below Power-On Reset (V_{DD} < V_{POR})

When the voltage on V_{DD} is lower than the required voltage (V_{POR}) needed to internally pull the asserted output to GND, $\overline{RESET}$ is undefined and should not be relied upon for proper device function.

■ Application Information

The AME8505 device is designed to assert a $\overline{RESET}$ signal when either the SENSE pin voltage drops below V_{IT} or $\overline{MR}$ is driven low. The $\overline{RESET}$ output remains asserted for a user-adjustable time after both $\overline{MR}$ and SENSE voltages return above their respective thresholds.

Feature Description

The AME8505 device is designed to assert a $\overline{RESET}$ signal when either the SENSE pin voltage drops below V_{IT} or $\overline{MR}$ is driven low. The $\overline{RESET}$ output remains asserted for a user-adjustable time after both $\overline{MR}$ and SENSE voltages return above their respective thresholds. A broad range of voltage threshold and reset delay time options are available for the AME8505 device, allowing these devices to be used in a wide arrange of applications.

The ADJ-version AME8505 can be set to any voltage above 0.405V using an external resistor divider. Two preset delay times are also user-selectable: connecting the C_T pin to V_{DD} results in a 300ms reset delay, whereas leaving the C_T pin open yields a 20ms reset delay. In addition, connecting a capacitor between C_T and GND allows the designer to select any reset delay period from 1.25ms to 10s.

SENSE Input

The SENSE input provides a pin at which any system voltage can be monitored. If the voltage on this pin drops below V_{IT}, then $\overline{RESET}$ is asserted. The comparator has a built-in hysteresis to ensure smooth $\overline{RESET}$ sertions and de-assertions. It is good analog design practice to put a 1nF to 10nF bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitics.

The AME8505 device can be used to monitor any voltage rail down to 0.405V using the circuit shown in Figure.1

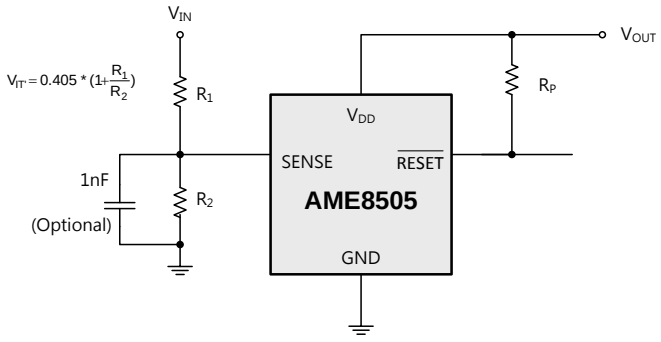


Figure.1 Using AME8505 device to Monitor a User-Defined Threshold Voltage

■ Application Information (Contd.)

Setting Reset Delay Time

The AME8505 has three options for setting the $\overline{\text{RESET}}$ delay time as shown in Figure.2.

Figure 2.1 shows the configuration for a fixed 300ms typical delay time by tying C_T to V_{DD}; a resistor from 40kΩ to 200kΩ must be used. Supply current is not affected by the choice of resistor.

Figure 2.2 shows a fixed 20ms delay time by leaving the C_T pin open.

Figure 3.3 shows a ground referenced capacitor connected to C_T for a user-defined program time between 1.25ms and 10s.

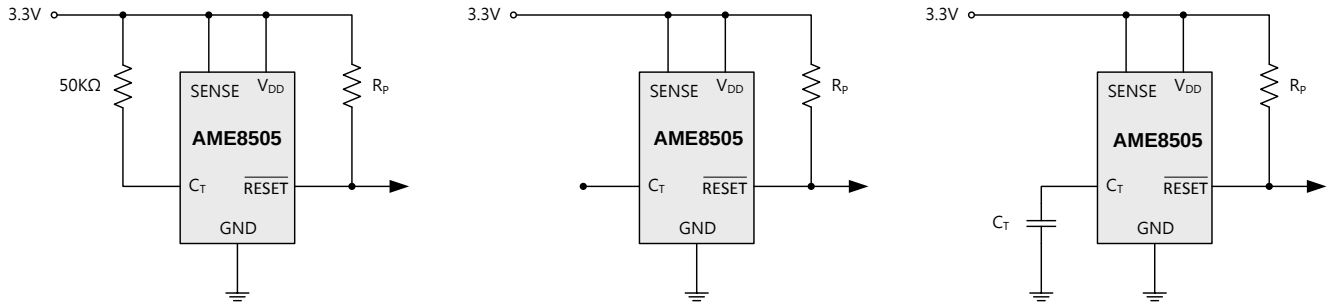


Figure.2 Configuration Used to Set the $\overline{\text{RESET}}$ Threshold Voltage

Manual Reset ($\overline{\text{MR}}$) Input

$\overline{\text{MR}}$ input allows a processor or other logic circuits to initiate a reset. A logic low ($0.3V_{DD}$) on $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to assert. After $\overline{\text{MR}}$ returns to a logic high and SENSE is above its reset threshold, $\overline{\text{RESET}}$ is de-asserted after the user-defined reset delay expires. Note that $\overline{\text{MR}}$ is internally tied to V_{DD} using a 90kΩ resistor, so this pin can be left unconnected if $\overline{\text{MR}}$ is not used.

See Figure.3 for how $\overline{\text{MR}}$ can be used to monitor multiple system voltages (e.g . I/O supply voltage of some Processors should be setup before core voltage and processor can only start after both I/O and core voltages setup). Note that if the logic signal driving $\overline{\text{MR}}$ does not go fully to V_{DD}, there is some additional current draw into V_{DD} as a result of the internal pull-up resistor on $\overline{\text{MR}}$.

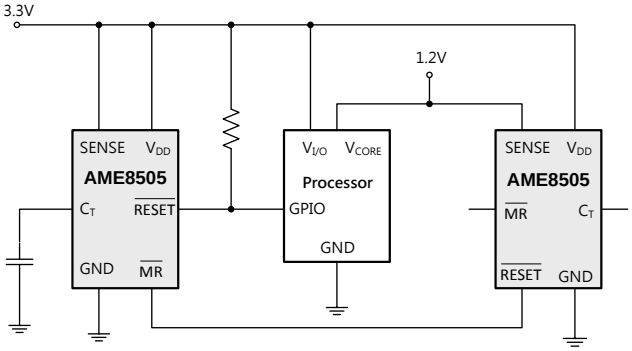


Figure.3

■ Application Information (Contd.)

To minimize current draw, a logic-level FET can be used as illustrated in Figure.4.

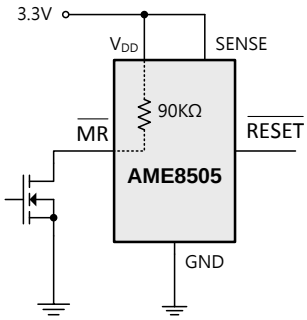


Figure.4 Using an External MOSFET to Minimize I_{DD} When $\overline{MR}$ Signal Does Not Go to V_{DD}

$\overline{RESET}$ Output

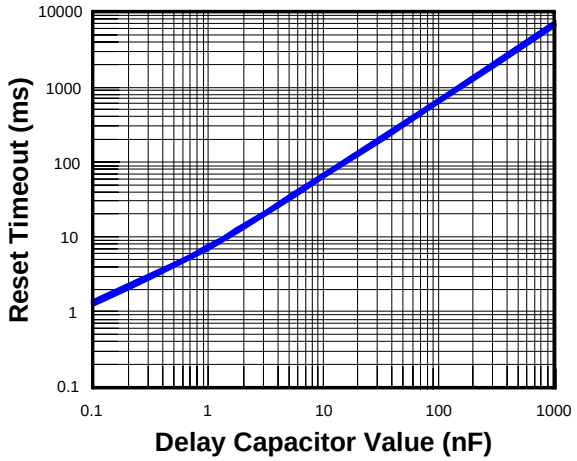
The $\overline{RESET}$ output is typically connected to the $\overline{RESET}$ control pin of a microprocessor. For Open−Drain output versions, a pull−up resistor must be used to hold this line high when $\overline{RESET}$ is not asserted. The $\overline{RESET}$ output is active once V_{DD} is over $V_{DD(min)}$, this voltage is much lower than most microprocessors' functional voltage range.

$\overline{RESET}$ remains high as long as SENSE is above its threshold (V_{IT}) and the $\overline{MR}$ input is logic high. If either SENSE falls below V_{IT} or $\overline{MR}$ is driven low, $\overline{RESET}$ is asserted.

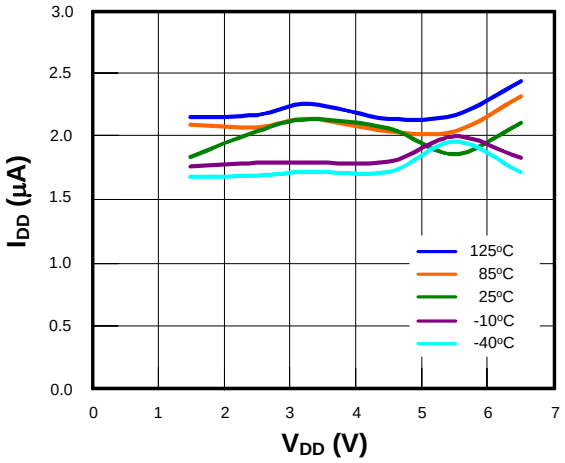
Once $\overline{MR}$ is again logic high and SENSE is above (V_{IT} +V_{HYS}), the $\overline{RESET}$ pin goes to a high impedance state after delay time (t_D). The open−drain structure of $\overline{RESET}$ is capable to allow the reset signal for the microprocessor to have a voltage higher than V_{DD} (up to 5.5V). The pull−up resistor should be no smaller than 10 kΩ as a result of the finite impedance of the $\overline{RESET}$ line.

■ Characterization Curve

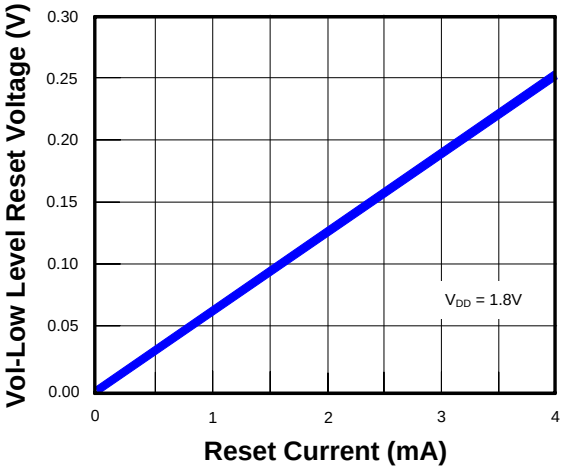
Reset Timeout vs. C_T



Supply Current vs. Supply Voltage

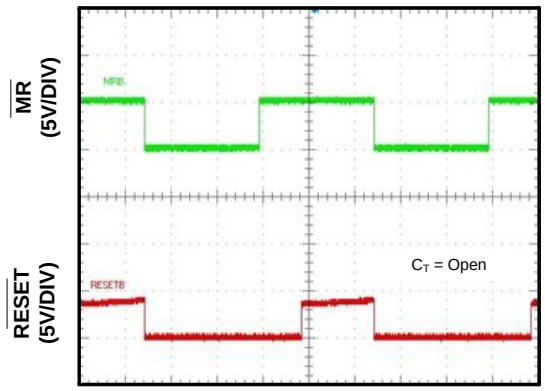


Low-Level Reset Voltage vs. Reset Current



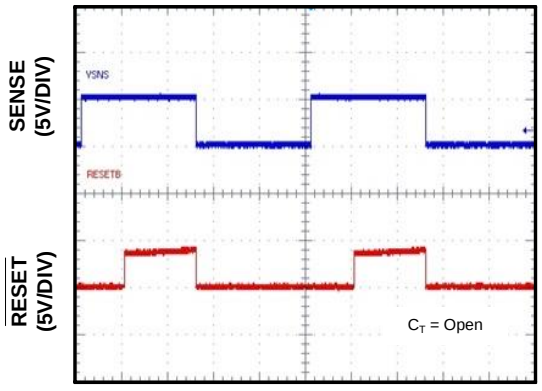
■ Characterization Curve (Contd.)

$\overline{MR}$ vs. $\overline{RESET}$ Timing



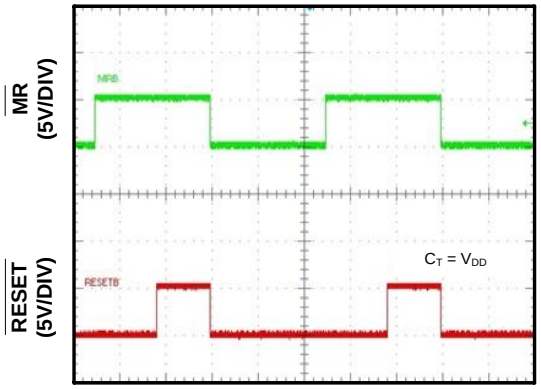
Time (20ms/DIV)

SENSE vs. $\overline{RESET}$ Timing



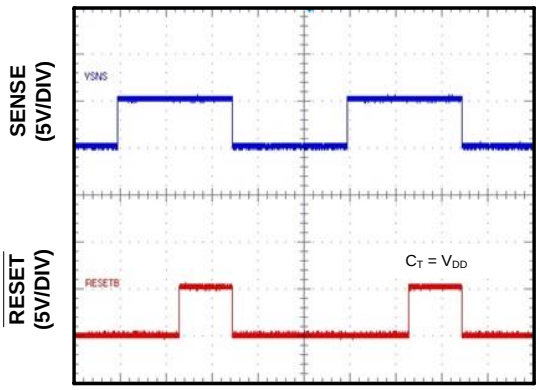
Time (20ms/DIV)

$\overline{MR}$ vs. $\overline{RESET}$ Timing



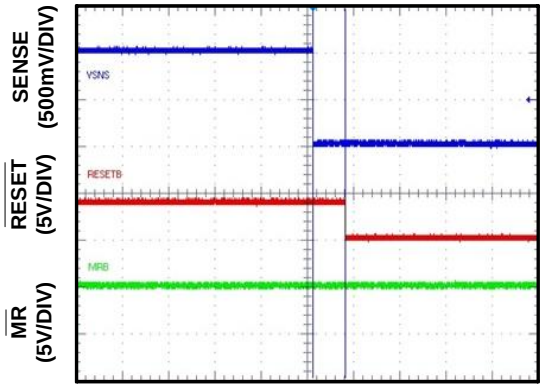
Time (200ms/DIV)

SENSE vs. $\overline{RESET}$ Timing



Time (200ms/DIV)

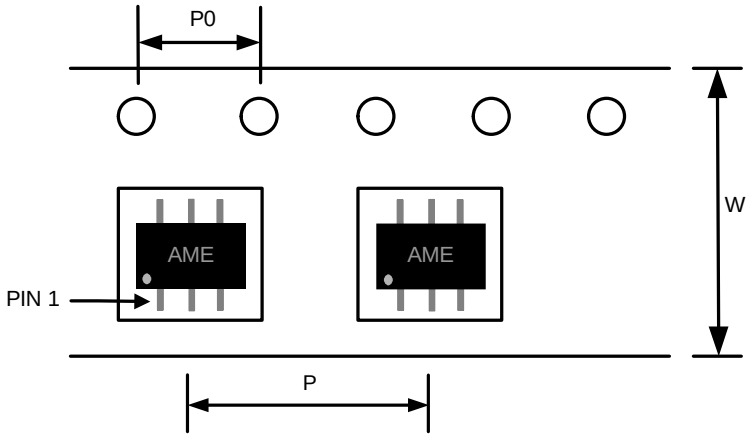
High to Low Level RESET Delay



Time (10μs/DIV)

■ Tape and Reel Dimension

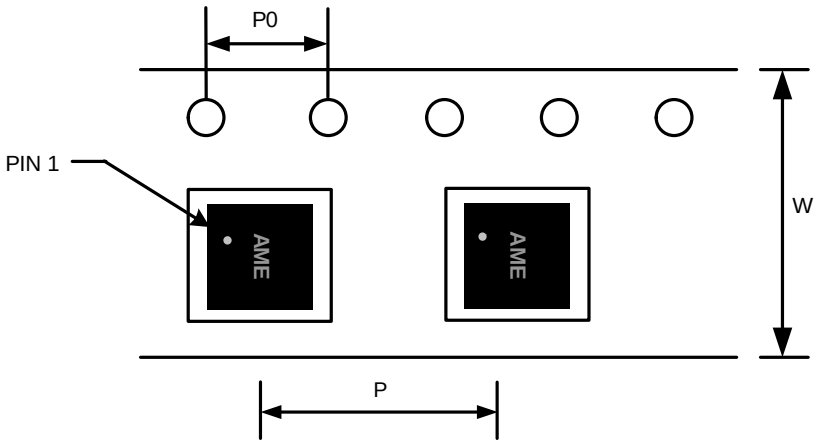
SOT-26



Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Pitch (P0)	Part Per Full Reel	Reel Size
SOT-26	8.0±0.1 mm	4.0±0.1 mm	4.0±0.1 mm	3000pcs	180±1 mm

DFN-6D
(2x2x0.75mm)

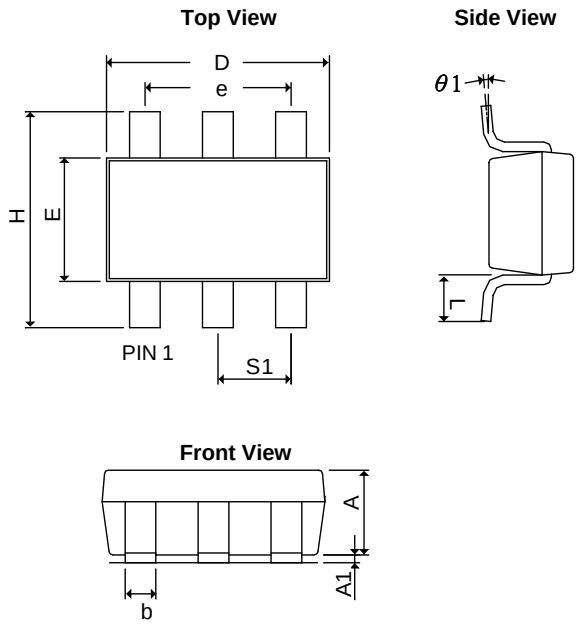


Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Pitch (P0)	Part Per Full Reel	Reel Size
DFN-6D	8.0±0.1 mm	4.0±0.1 mm	4.0±0.1 mm	3000pcs	180±1 mm

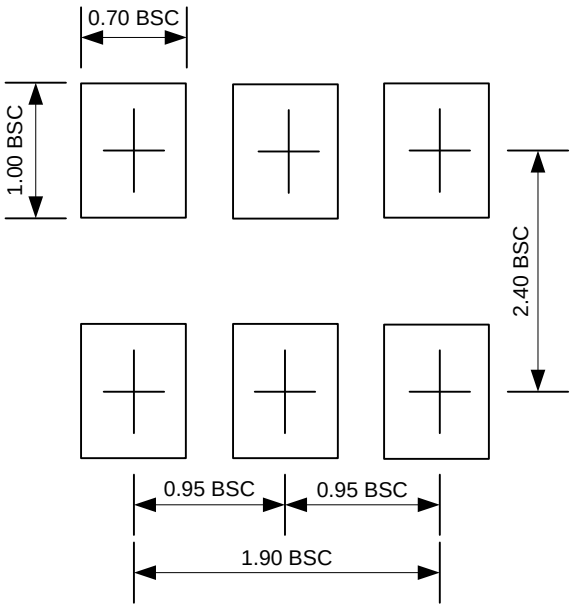
■ Package Dimension

SOT-26



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.30	0.0354	0.0512
A_1	0.00	0.15	0.0000	0.0059
b	0.30	0.55	0.0118	0.0217
D	2.70	3.10	0.1063	0.1220
E	1.40	1.80	0.0551	0.0709
e	1.90 BSC		0.0748 BSC	
H	2.60	3.00	0.1024	0.1181
L	0.37 BSC		0.0146 BSC	
θ1	0^o	10^o	0^o	10^o
S_1	0.95 BSC		0.0374 BSC	

■ Lead Pattern

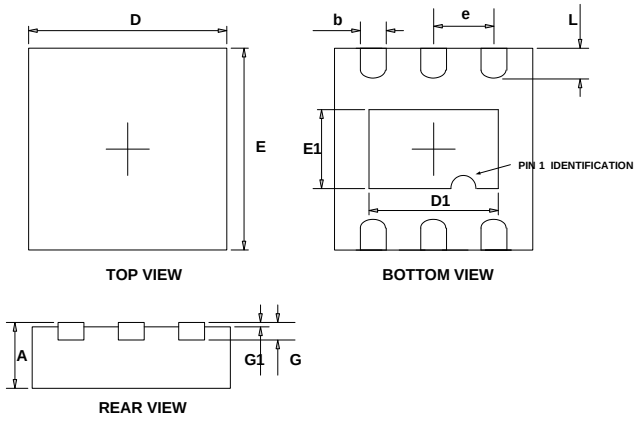


Note:

1. Lead pattern unit description:
   BSC: Basic. Represents theoretical exact dimension or dimension target.
2. Dimensions in Millimeters.
3. General tolerance ±0.05mm unless otherwise specified.

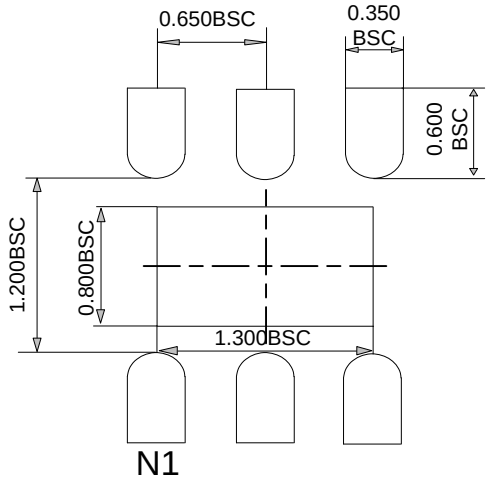
■ Package Dimension (Contd.)

DFN-6D
(2x2x0.75mm)



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
e	0.650TYP		0.026TYP	
D1	1.100	1.650	0.043	0.065
E1	0.600	1.050	0.024	0.041
b	0.180	0.350	0.007	0.014
L	0.200	0.450	0.008	0.018
G	0.178	0.228	0.007	0.009
G1	0.000	0.050	0.000	0.002

■ Lead Pattern



Note:

1. Lead pattern unit description:
   BSC: Basic. Represents theoretical exact dimension or dimension target.
2. Dimensions in Millimeters.
3. General tolerance ±0.05mm unless otherwise specified.

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