5.5V 500mA, High PSRR Linear Regulator

■ General Description

The AME8903 is CMOS LDO regulator sourcing 500mA output current. The input voltage is as low as 1.4V and the output voltage can be set from 0.8V. The device consume 40µA of quiescent current (no load).

EN pin input logic level to control ON/OFF of the output voltage. The features low noise, high PSRR and good line/load transient. The device support protection such as over-load, short circuit and overheating.

■ Features

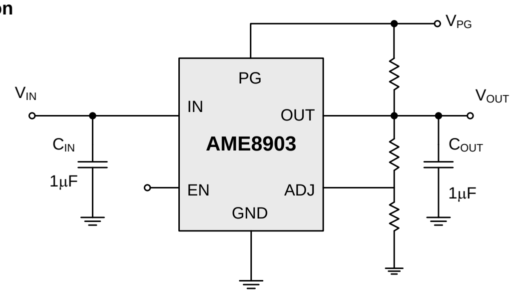
- Operating Input Voltage: 1.4V to 5.5V
- Adjustable Output Voltage: 0.8V to 5V
- Fixed Output Voltage: 0.8V to 4.5V(0.1V steps)
- Quiescent Current: 40µA(typ.)
- Low Dropout : 120mV(typ.) @0.5A,V_{OUT} = 2.5V
- Output Voltage Accuracy : ± 0.8%(V_{OUT} > 1.8V)
- Stable with Small 1µF Ceramic Capacitors
- Over-Current Protection
- Thermal Shutdown Protection : 160^{o}C
- Auto Output Discharge Function
- Available in SOT-25 & DFN-6G(1.2x1.2x0.37mm) & DFN-6D(2x2x0.75mm) Packages
- RoHS, Halogen Free and TSCA Compliance

■ Application

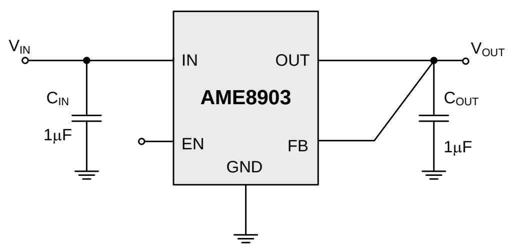
- Laptop, AIO, Mini PC
- Battery Powered Equipment
- Portable Communication Equipment
- Cameras, Image Sensors and Camcorders

■ Typical Application Schematic

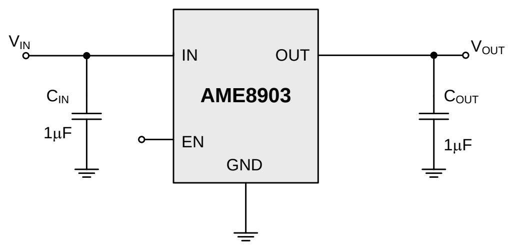
ADJ Version



Fix Version- with V_{FB}

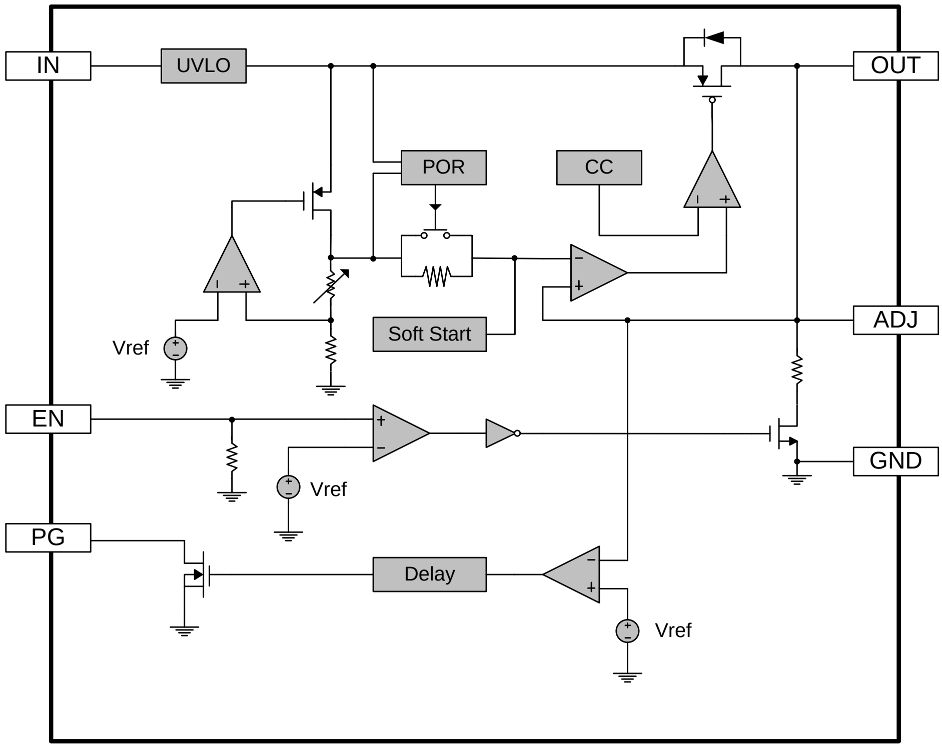


Fix Version – without V_{FB}

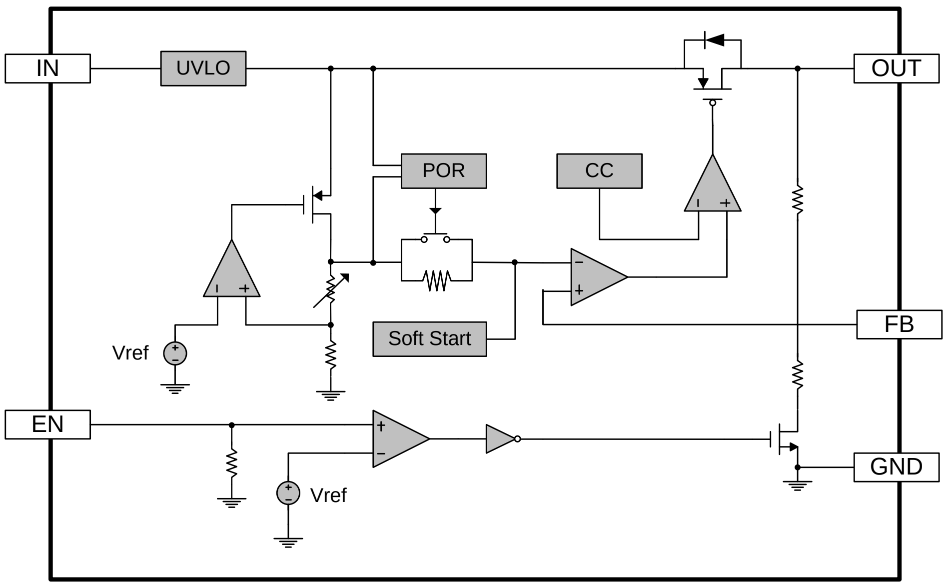


■ Function Block Diagram

ADJ Version

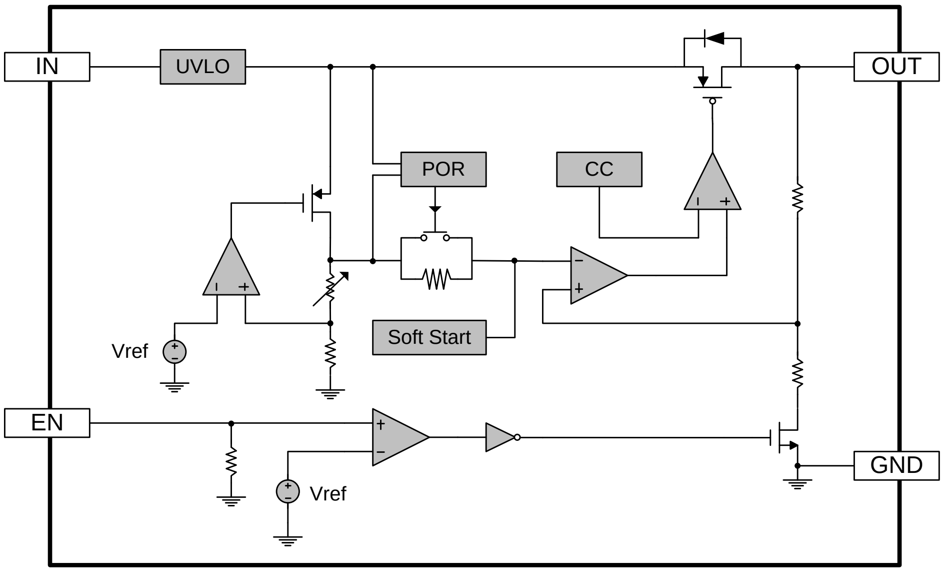


Fix Version – with V_{FB}



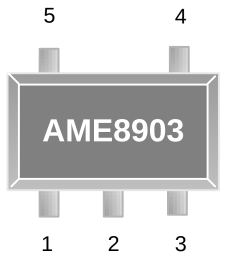
■ Function Block Diagram (Contd.)

Fix Version – without V_{FB}



Pin Configuration

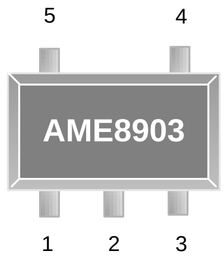
SOT-25
Top View



AME8903-AEVxxx

1. IN
2. GND
3. EN
4. NC
5. OUT

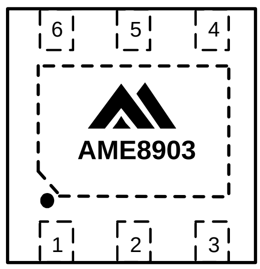
SOT-25
Top View



AME8903-DEVADJ

1. IN
2. GND
3. EN
4. ADJ
5. OUT

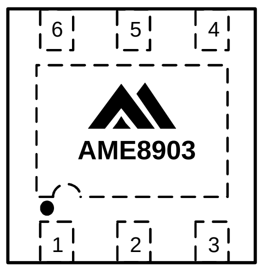
DFN-6G
(1.2x1.2x0.37mm)
Top View



AME8903-AVYxxx

1. OUT
2. FB
3. GND
4. EN
5. NC
6. IN

DFN-6D
(2x2x0.75mm)
Top View



AME8903-DVYADJ

1. OUT
2. ADJ
3. GND
4. EN
5. PG
6. IN

Pin Description

Pin Number				I/O	Pin Name	Pin Description
SOT-25		DFN-6G	DFN-6D			
A	D	A	D			
5	5	1	1	O	OUT	LDO Output pin
NA	4	2	2	I	ADJ/FB	Feedback Input pin
2	2	3	3	NA	GND	Ground pin
3	3	4	4	I	EN	Chip Enable Input pin (Active High)
4	NA	5	NA	NA	NC	Not Internally Connected.
1	1	6	6	I	IN	Power Supply Input pin
NA	NA	NA	5	O	PG	Power Good pin
NA	NA	EPAD	EPAD	NA	EPAD	Recommend to connect the EPAD to GND, but leaving it open is also acceptable.

■ Ordering Information

AME 8903 - x x x xxx xx

- **Tape & Reel (Note1)**
- **Output Voltage**
- **Number of Pins**
- **Package Type**
- **Pin Configuration**

Pin Configuration		Package Type	Number of Pins	Output Voltage
A	1. IN	E: SOT-2X	V: 5	100: 1.0V
(SOT-25)	2. GND	V: DFN	Y: 6	120: 1.2V
	3. EN			180: 1.8V
	4. NC			280: 2.8V
	5. OUT			300: 3.0V
				330: 3.3V
D	1. IN			ADJ: ADJ
(SOT-25)	2. GND			
	3. EN			
	4. ADJ			
	5. OUT			
A	1. OUT			
(DFN-6G)	2. FB			
	3. GND			
	4. EN			
	5. NC			
	6. IN			
D	1. OUT			
(DFN-6D)	2. ADJ			
	3. GND			
	4. EN			
	5. PG			
	6. IN			

Note1: For DFN package only, please refer to AME8903 Available Option or consult AME sales office or authorized Rep. / Distributor for detail information.

■ Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Input Voltage	V_{IN}	-0.3 to +6	V
Output Voltage	V_{OUT}	-0.3 to +6	
Enable Voltage	V_{EN}	-0.3 to +6	
FB/ADJ Pin		-0.3 to +6	
Power Good Pin		-0.3 to +6	
ESD Classification	HBM	±4000	V
	MM	±200	
	CDM	±1000	

■ Recommended Operation Conditions

Parameter	Symbol	Value	Unit
Input Voltage Range	V_{IN}	1.4 to 5.5	V
Fix OUTPUT Voltage Range	V_{OUT}	0.8 to 4.5	
ADJ OUTPUT Voltage Range	V_{OUT}	0.8 to 5	
Ambient Temperature Range	T_A	-40 to +85	^oC
Junction Temperature Range	T_J	-40 to +125	
Storage Temperature	T_{STG}	-55 to +150	

■ Thermal Information

Parameter	Package	Die Attach	Symbol	Maximum	Unit
Thermal Resistance* (Junction to Case)	SOT-25	Conductive Epoxy	θ_{JC}	81	^oC / W
	DFN-6D	Conductive Epoxy		16	
	DFN-6G	Non-Conductive Epoxy		68	
Thermal Resistance (Junction to Ambient)	SOT-25	Conductive Epoxy	θ_{JA}	260	
	DFN-6D	Conductive Epoxy		66	
	DFN-6G	Non-Conductive Epoxy		167	
Internal Power Dissipation	SOT-25	Conductive Epoxy	P_D	400	mW
	DFN-6D	Conductive Epoxy		1515	
	DFN-6G	Non-Conductive Epoxy		600	
Lead Temperature (soldering 10 sec)**				300	^oC

* Measure θ_{JC} on backside center of Exposed Pad.

** MIL-STD-202G210F

■ Electrical Specifications

V_{IN} = $V_{OUT-NOM}$ + 0.5V and V_{IN} > 1.6V, V_{EN} = 1.2V, I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1.0µF, T_J = 25°C.

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output Voltage Accuracy	$V_{OUT-ACC}$	V_{OUT} ≧ 2.5V		-1		1	%
		2.5V > V_{OUT} ≧ 1.8V		-0.8		0.8	%
		V_{OUT} < 1.8V		-20		20	mV
ADJ Reference Voltage	V_{ADJ}	I_{OUT} = 1mA		0.792	0.8	0.808	V
Line Regulation	REG_{LINE}	V_{IN} = $V_{OUT-NOM}$ + 0.5V to 5.25V, V_{IN} ≧ 1.4V			0.02	0.1	%/V
Load Regulation	REG_{LOAD}	I_{OUT} = 1mA to 500mA			0.5	10	mV
Dropout Voltage	V_{DROP}	I_{OUT} = 500mA	V_{OUT} < 1.05V		Note2		
			1.05V ≦ V_{OUT} < 1.2V		585	750	mV
			1.2V ≦ V_{OUT} < 1.5V		420	570	mV
			1.5V ≦ V_{OUT} < 1.8V		295	400	mV
			1.8V ≦ V_{OUT} < 2.1V		200	275	mV
			2.1V ≦ V_{OUT} < 2.5V		150	230	mV
			2.5V ≦ V_{OUT} < 3.0V		120	190	mV
			3.0V ≦ V_{OUT}		90	165	mV
Quiescent Current	I_Q	V_{EN} = V_{IN}, I_{OUT} = 0mA			40	75	µA
Shutdown Current	I_{SHDN}	V_{EN} = 0V			0.05	1	µA
Output Current Limit	I_{LIM}	V_{OUT} = 90% of $V_{OUT-NOM}$		520			mA
Short Circuit Current	I_{SC}	V_{OUT} = 0V			100		mA
Enable High Level	V_{EN-HI}	V_{IN} = 5V		1			V
Enable Low Level	V_{EN-LO}	V_{IN} = 5V				0.4	V
Enable Input Current	I_{EN}	V_{EN} = V_{IN} = 5.5V			0.15	0.6	µA
Output Discharge Resistance	R_{DSG}				60		Ω
Power Supply Ripple Rejection	PSRR	I_{OUT} = 30mA, f = 1KHz			75		dB
		I_{OUT} = 30mA, f = 100KHz			60		dB
		I_{OUT} = 30mA, f = 1MHz			50		dB
		I_{OUT} = 30mA, f = 10MHz			50		dB

Note2: For V_{OUT} below 1.05V, Dropout Voltage is the V_{IN-MIN} to Output Differential.

■ Electrical Specifications (Contd.)

$V_{IN} = V_{OUT\text{-}NOM} + 0.5V$ and $V_{IN} > 1.6V$, $V_{EN} = 1.2V$, $I_{OUT} = 1mA$, $C_{IN} = C_{OUT} = 1.0\mu F$, $T_J = 25^oC$.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output Noise	eN	f = 10Hz to 100KHz		36		μV_{RMS}
PG Threshold Voltage		V_{OUT} Rising		90		%
PG Hysteresis		V_{OUT} Falling		10		%
PG Low Voltage		PG sinks 1mA		0.1	0.2	V
PG Delay Time				1.1		ms
Over Temperature Shutdown	OTS			160		^oC
Over Temperature Hysteresis	OTH			35		^oC

■ Application Information

Input Capacitor

Bypass capacitor is placed to improve AC performance and recommended from IN to GND due to low impedance path. It is recommend to be adopted for reliable performance over temperature range by the X7R or X5R capacitor. A 1μF or greater capacitor locates as close as possible to AME8903.

The ESR is not required but it is recommended to use a ceramic capacitor for its low ESR and ESL. A good input capacitor will ease the influence of input trace inductance and source resistance during load current changes.

Output Capacitor

It is required to fulfill both requirements for minimum amount of capacitance and ESR in all LDOs application by output capacitor. The LDO requires an output capacitor connected as close as possible to the output and ground pins.

The AME8903 specifically work with low ESR ceramic output capacitor in space-saving and performance consideration. The recommended capacitor value is 1uF, ceramic X7R or X5R type due to its low capacitance variations over the specified temperature range. The ESR of output capacitor relates to stability and the maximum ESR should be less than 0.5Ω.

Larger output capacitance is able to reduce noise and enhance load transient response, stability, and PSRR. When selecting the capacitor the changes with temperature, DC bias and package size needs to be required. Especially for small package size capacitors such as 0201 the effective capacitance drops rapidly with the applied DC bias voltage. Only ceramic capacitors are recommended due to low ESR, the other types like tantalum capacitors are not.

Enable

Shutdown mode: If the EN pin voltage is < 0.4V, AME8903 is disabled and its pass transistor is turned off. The active discharge transistor is active so the output voltage is pulled to GND through typical 60Ω resistor.

Operation mode: If the EN pin voltage is > 1.0V, AME8903 is enabled and regulates the output voltage. The active discharge transistor is turned off.

The EN pin has internal pull−down current source with value of 0.15μA typ. which assures the device is turned off when the EN pin is unconnected. In case when the EN function isn't required the EN pin should be tied directly to IN pin.

Output Current Limit

Output current is internally limited to a 520mA min. The LDO will source this current when the output voltage drops down from the nominal output voltage (test condition is $V_{OUT\text{-}NOM}$ – 100mV). If the output voltage is shorted to ground, the short circuit protection will limit the output current to 100mA Typ. The current limit and short circuit protection will work properly over the whole temperature and input voltage ranges. There is no limitation for the short circuit duration.

Reverse Current

When $V_{OUT} > V_{IN}$, body diode of PMOS will be forward biased. In the case, extended reverse current condition can be anticipated and the device may require additional external protection.

Enable Turn-On Time

Defined as the time from EN assertion to the point where V_{OUT} will reach 98% of its nominal value. This time is dependent on various application conditions such as $V_{OUT\text{-}NOM}$, C_{OUT} and T_A.

Power Supply Rejection Ratio (PSRR)

The AME8903 features high PSRR. The PSRR at higher frequencies (in the range above 100 kHz) can be tuned by the selection of C_{OUT} capacitor and proper PCB layout. A simple LC filter could be added to the AME8903's IN pin for further PSRR improvement.

■ Application Information (Contd.)

Thermal Shutdown

This feature prevents overheating from damaging to IC due to application failure. When the LDO's die temperature exceeds the thermal shutdown threshold value, AME8903 is internally disabled. The AME8903 will remain in this state until the die temperature decreases by value called thermal shutdown hysteresis. Once the IC temperature falls this way the LDO is back enabled.

Power Dissipation (P_D)

P_D induced by voltage drop across PMOS and by the output current flowing through AME8903 needs to be dissipated out from the chip. The maximum power dissipation ($P_{D(MAX)}$) is dependent on the PCB layout, number of used Cu layers, Cu layers thickness and the ambient temperature.

The maximum power dissipation can be calculated by following equation:

$$P_{D(MAX)} = \frac{T_J - T_A}{\theta_{JA}} \text{ [W]}$$

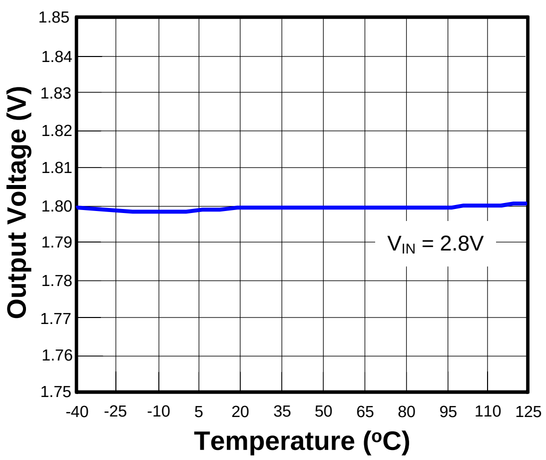
Where ($T_J - T_A$) is the temperature difference between the junction and ambient temperatures and θ_{JA} is the thermal resistance (dependent on the PCB as mentioned above).

$$P_D = V_{IN} \cdot I_{GND} + (V_{IN} - V_{OUT}) \cdot I_{OUT} \text{[W]}$$

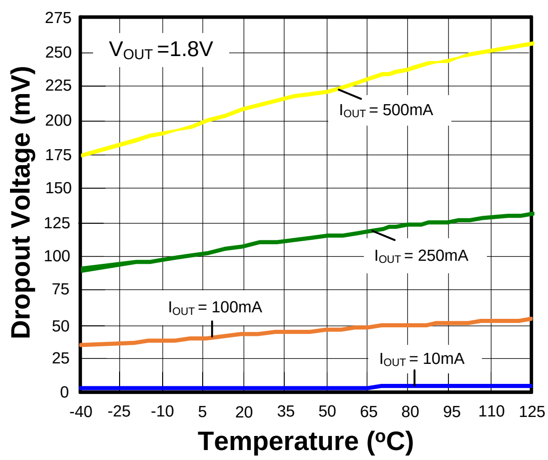
Where I_{GND} is the AME8903's ground current, which is dependent on the output load current. Connecting the exposed pad and N/C pin to a large ground planes helps to dissipate the heat from the chip.

■ Characterization Curve

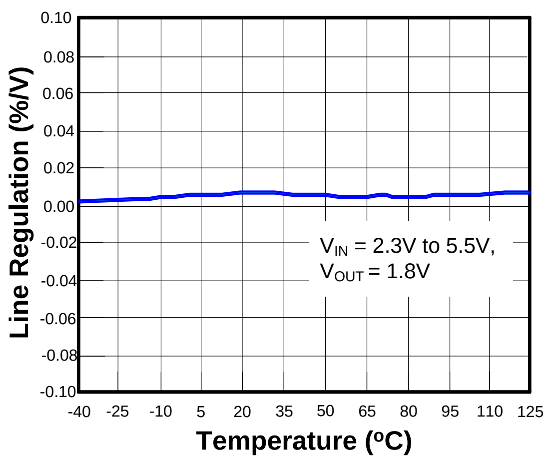
Output Voltage vs. Temp.



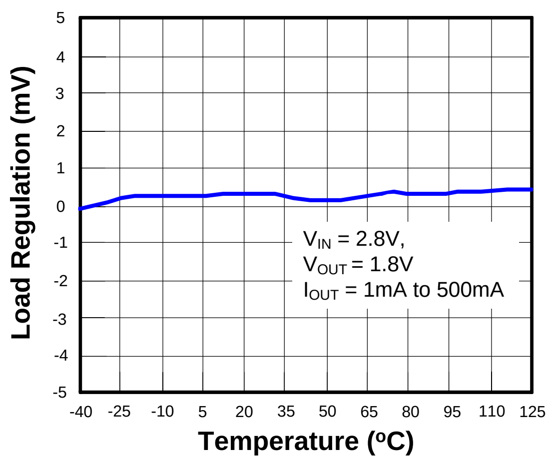
Dropout Voltage vs. Temp.



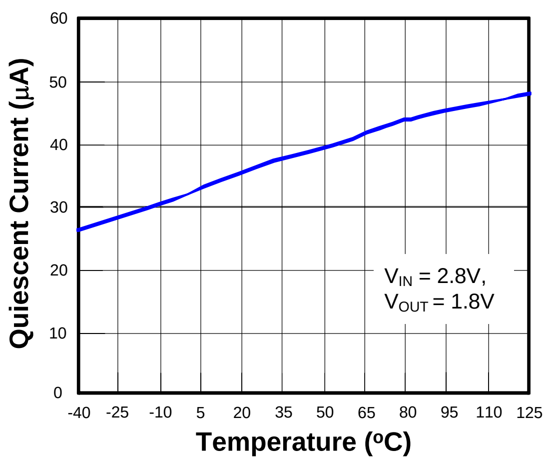
Line Regulation vs. Temp.



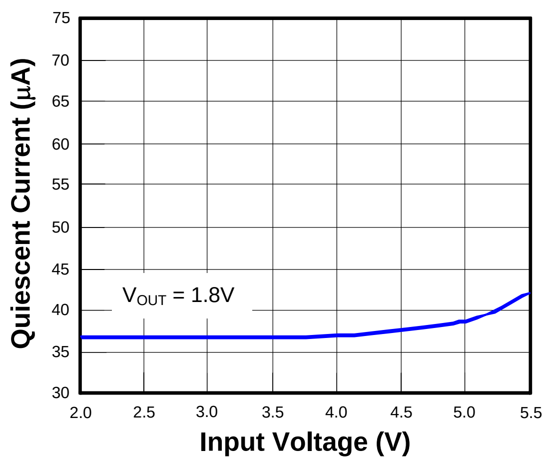
Load Regulation vs. Temp.



IQ vs. Temp.

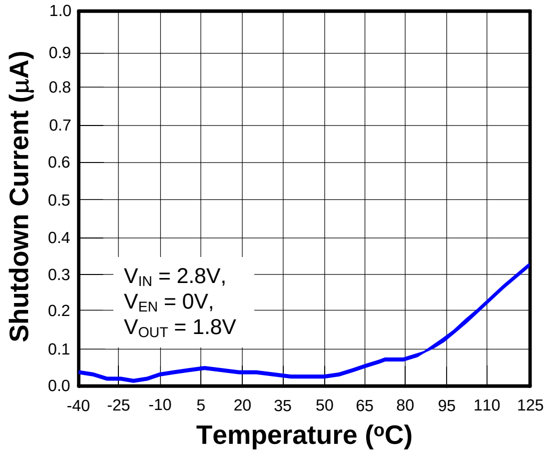


IQ vs. Input Voltage

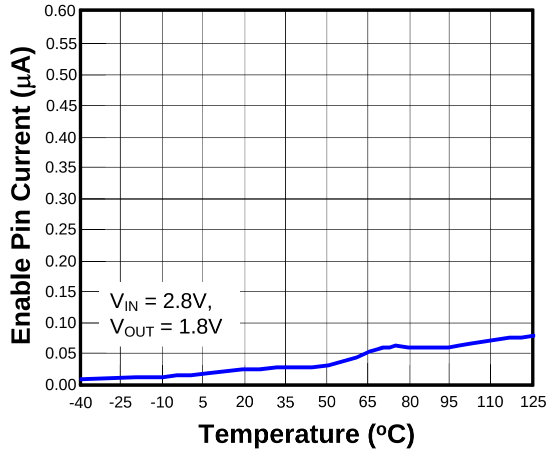


■ Characterization Curve (Contd.)

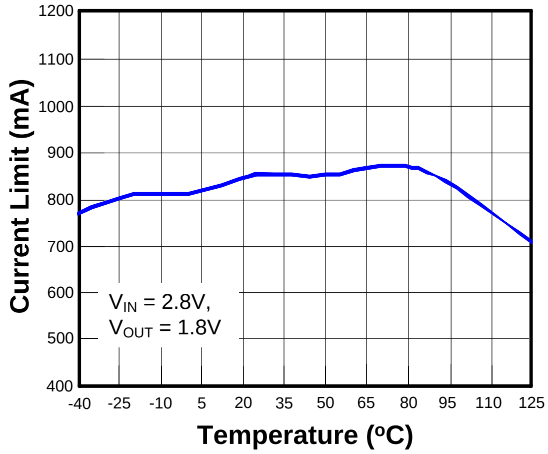
I_{SHDN} vs. Temp.



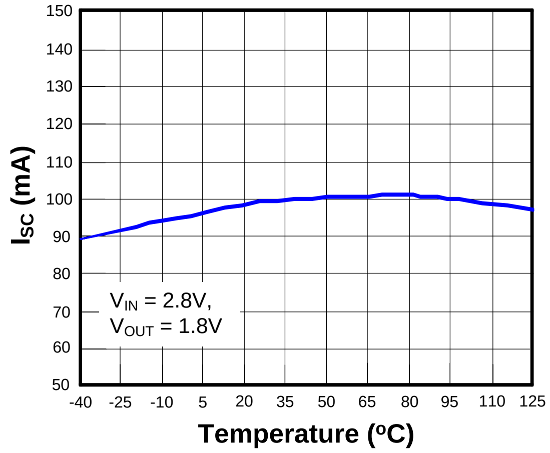
Enable Current vs. Temp.



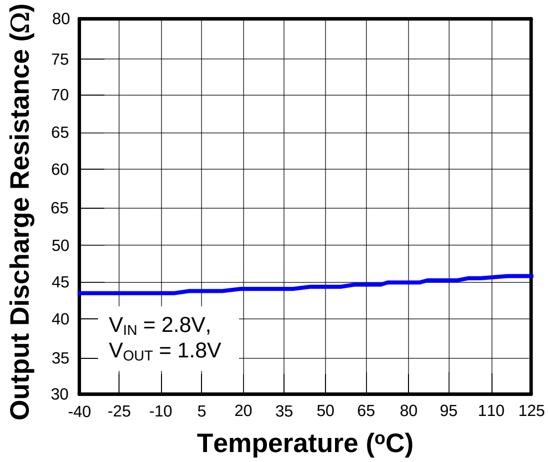
Current Limit vs. Temp.



Short Circuit Current vs. Temp.

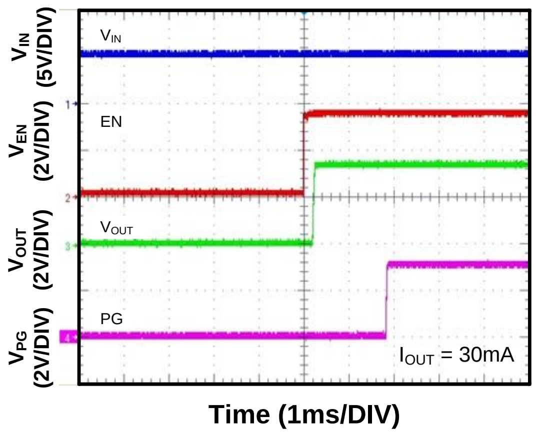


R_{DSG} vs. Temp.

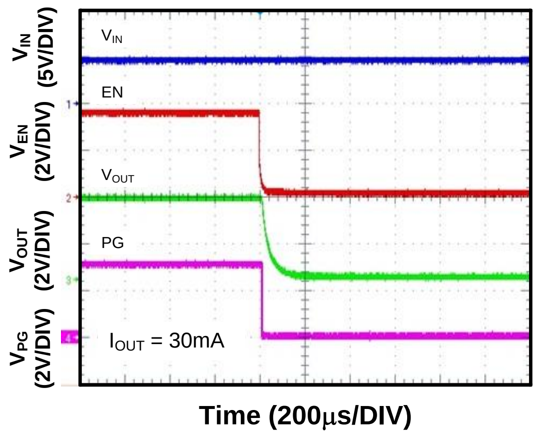


■ Characterization Curve (Contd.)

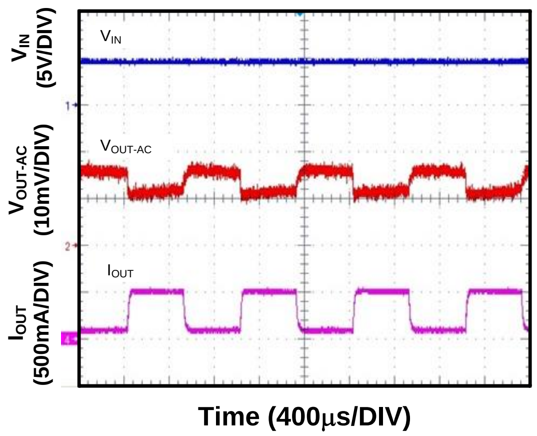
Start-Up from Enable



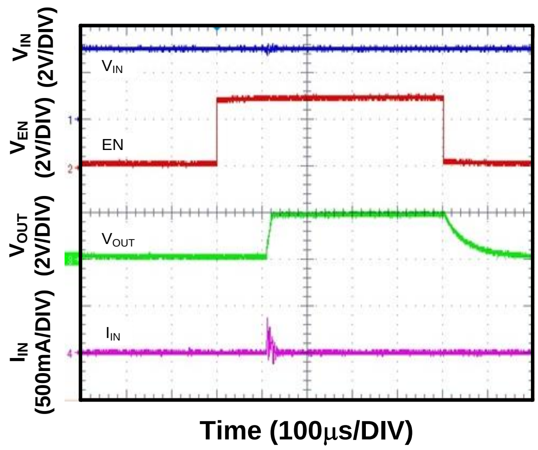
Shutdown from Disable



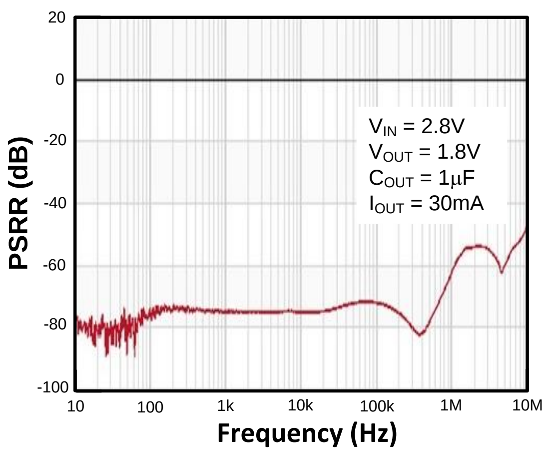
Load Transient Response



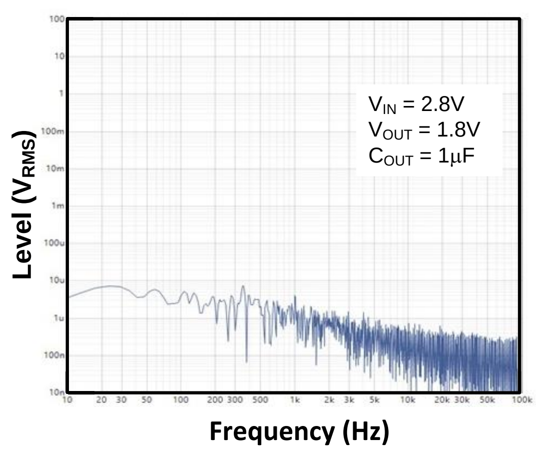
Turn-On/Off – EN Driven



Power Supply Rejection Ration

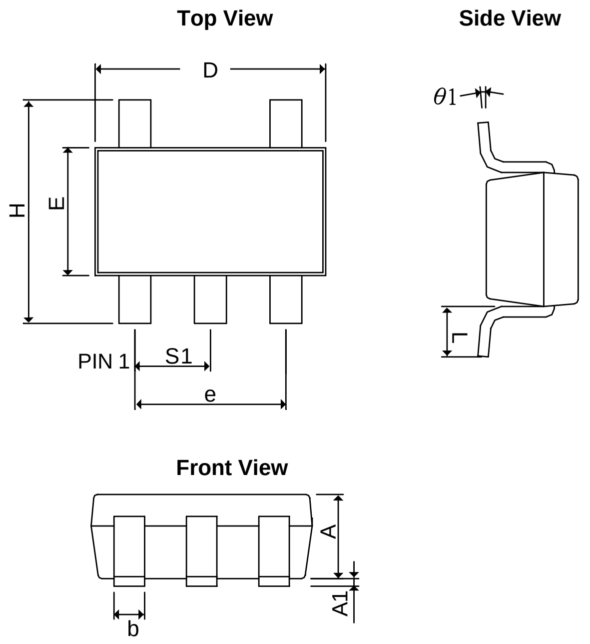


Output Voltage Noise Spectral



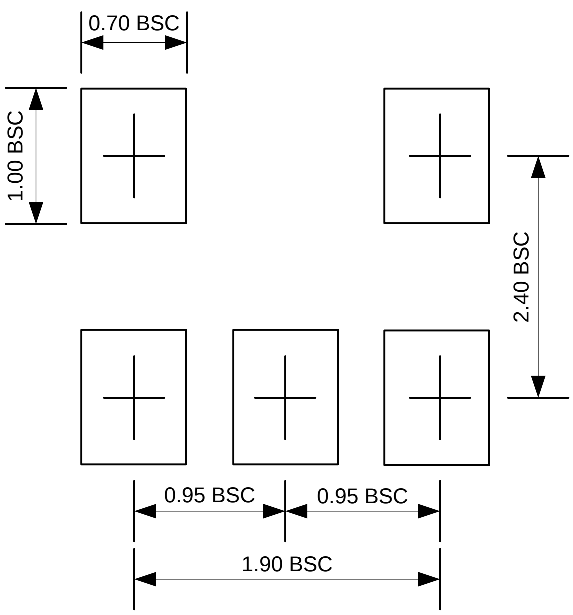
■ Package Dimension

SOT-25



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.30	0.0354	0.0512
A_1	0.00	0.15	0.0000	0.0059
b	0.30	0.55	0.0118	0.0217
D	2.70	3.10	0.1063	0.1220
E	1.40	1.80	0.0551	0.0709
e	1.90 BSC		0.0748 BSC	
H	2.60	3.00	0.1024	0.1181
L	0.37 BSC		0.0146 BSC	
θ1	0^o	10^o	0^o	10^o
S_1	0.95 BSC		0.0374 BSC	

■ Lead Pattern

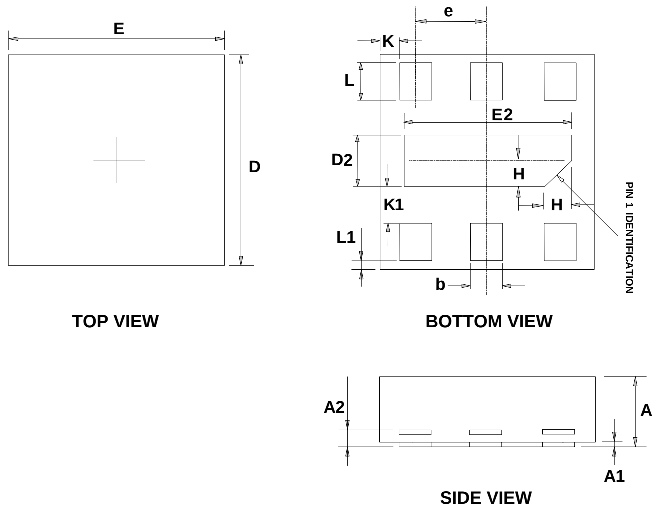


Note:

1. Lead pattern unit description:
   BSC: Basic. Represents theoretical exact dimension or dimension target.
2. Dimensions in Millimeters.
3. General tolerance ±0.05mm unless otherwise specified.

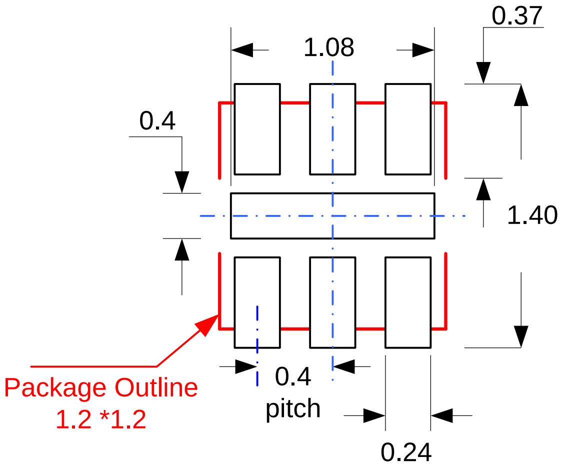
■ Package Dimension (Contd.)

DFN-6G(1.2x1.2x0.37mm)



SYMBOLS	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.340	0.370	0.400	0.013	0.015	0.016
A1	0.000	0.020	0.050	0.000	0.001	0.002
A2	0.100 REF			0.004 REF		
b	0.130	0.180	0.230	0.005	0.007	0.009
D	1.150	1.200	1.250	0.045	0.047	0.049
E	1.150	1.200	1.250	0.045	0.047	0.049
D2	0.250	0.300	0.350	0.010	0.012	0.014
E2	0.890	0.940	0.990	0.035	0.037	0.039
e	0.300	0.400	0.500	0.012	0.016	0.020
H	0.150REF			0.006 REF		
K	0.110REF			0.004 REF		
K1	0.150	0.200	0.250	0.006	0.008	0.010
L	0.150	0.200	0.250	0.006	0.008	0.010
L1	0.000	0.050	0.100	0.000	0.002	0.004

■ Lead Pattern

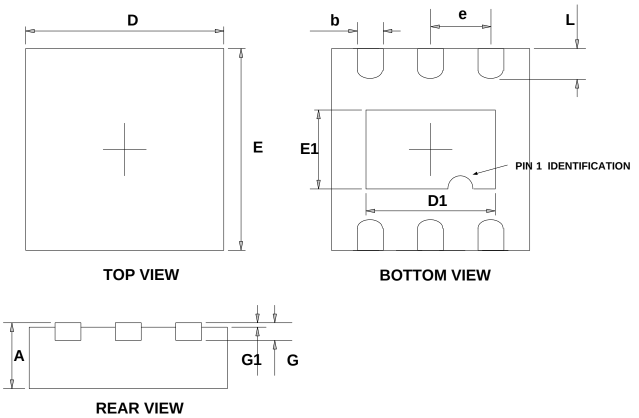


Note:

1. Dimensions in Millimeters.

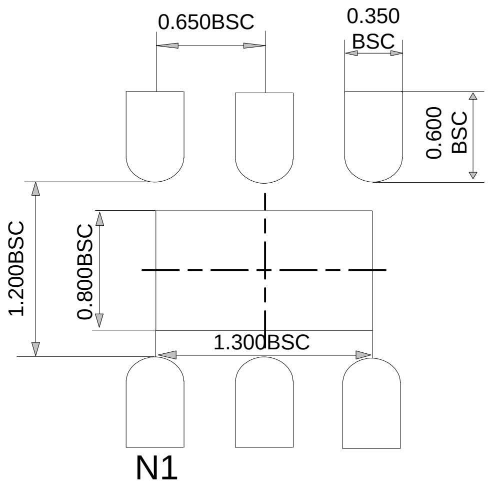
■ Package Dimension (Contd.)

DFN-6D(2x2x0.75mm)



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
e	0.650 TYP		0.026 TYP	
D1	1.100	1.650	0.043	0.065
E1	0.600	1.050	0.024	0.041
b	0.180	0.350	0.007	0.014
L	0.200	0.450	0.008	0.018
G	0.178	0.228	0.007	0.009
G1	0.000	0.050	0.000	0.002

■ Lead Pattern



Note:

1. Dimensions in Millimeters.
2. General tolerance ±0.05mm unless otherwise specified.

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