■ General Description

The AME5242 is a specific 40V HV buck converter that operates in either CV/CC mode supports an output voltage range of 0.8V to 12V and support constant output current at 200KHz switching frequency. AME5242 integrated auto detection USB devices plugged in, providing the correct hand-shaking protocol with compliant client devices. This product is specifically designed for car charger or wall adapter application.

The AME5242 supports the following charging logic schemes:

- USB 2.0 BC1.2
- Chinese Telecom Standard YD/T 1591-2009
- Divider Mode, compliant with Apple devices

Protection features include under voltage protection, over voltage protection, current limit, thermal shutdown, and short circuit protection. The device is available in SOP-8/PP package with exposed pad for low thermal resistance.

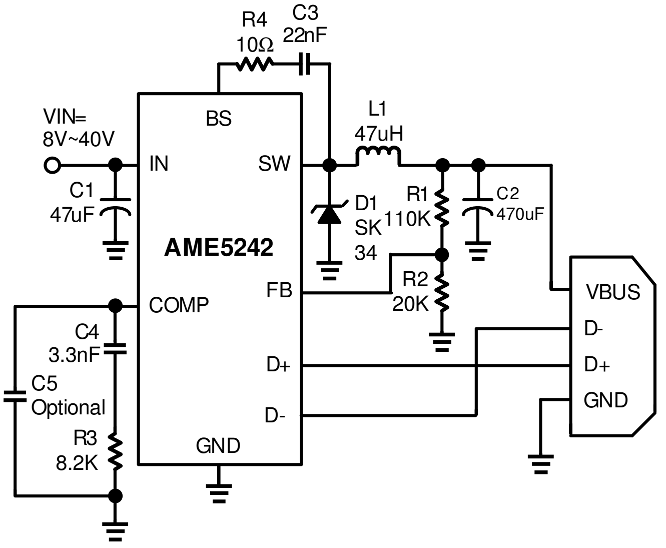
■ Features

- 40V Maximum Rating for Input Power
- Support Fast Charge of Most Apple Devices and BC1.2 and YD/T 1591-2009 Complaint Devices
- Auto Detection of USB Devices Plugged in
- 200KHz Switching Frequency
- CC/CV Mode Function
- Internal Soft Start
- UVP, Input/Output OVP, OTP, SCP
- Available in SOP-8/PP Package
- RoHS Compliant and Halogen Free

■ Application

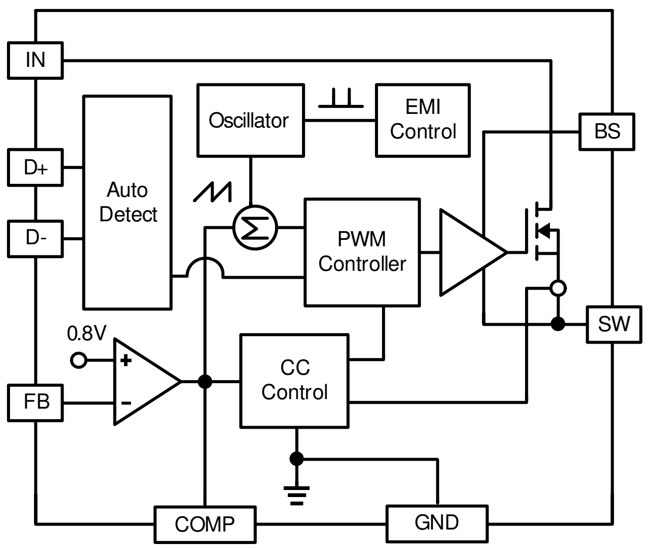
- Car Charger
- Wall Adapter

■ Typical Application



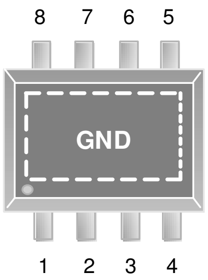
AME5242-AZAADJ-24

■ Functional Block Diagram



■ Pin Configuration

SOP-8/PP
Top View



AME5242-AZAADJ

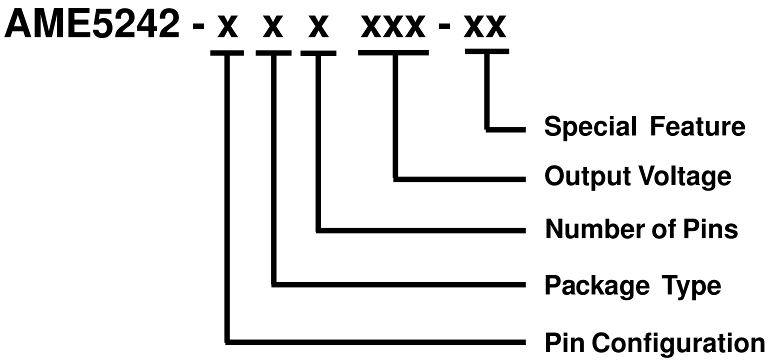
1. IN
2. COMP
3. D+
4. D-
5. FB
6. GND
7. SW
8. BS

*** Die Attach:**
Conductive Epoxy

■ Pin Description

Pin No.	Pin Name	Pin Description
1	IN	Input power.
2	COMP	Compensation Node.
3	D+	USB Data.
4	D-	USB Data.
5	FB	Feedback Input.
6	GND	Ground.
7	SW	Power Switching Output
8	BS	High Side. Gate Drive Boost Input.
9	Exposed Pad	Ground.

■ Ordering Information



Pin Configuration	Package Type	Number of Pins	Output Voltage	Special Feature
A (SOP-8/PP) 1. IN 2. COMP 3. D+ 4. D- 5. FB 6. GND 7. SW 8. BS	Z: SOP/PP	A: 8	ADJ: Adjustable	10 24

■ Absolute Maximum Ratings

Parameter		Maximum	Unit
Input Voltage		-0.3V to 40	V
Switch Voltage		-1 to V_{IN} +1	V
Boost Switch Voltage		V_{SW} - 0.3 to V_{SW} + 7	V
All Other Pins		-0.3V to 7	V
Electrostatic Discharge (HBM)		2000	V
Junction Temperature		150	°C
Storage Temperature		-65 to +150	°C
ESD Classification	HBM	2	kV
	MM	150	V

■ Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Input Voltage	V_{IN}	8 to 40	V
Output Voltage	V_{OUT}	0.8 to 12	
Junction Temperature Range	T_J	-40 to +125	°C
Ambient Temperature Range	T_A	-40 to +85	

■ Thermal Information

Parameter	Package	Die Attach	Symbol	Maximum	Unit
Thermal Resistance* (Junction to Case)	SOP-8/PP	Conductive Epoxy	θ_{JC}	19	°C / W
Thermal Resistance (Junction to Ambient)			θ_{JA}	84	
Internal Power Dissipation			P_D	1450	mW
Lead Temperature (soldering 10 sec)**				260	°C

* Measure θ_{JC} on backside center of molding compound if IC has no tab.

** MIL-STD-202G 210F

■ Electrical Specifications

Typical values V_{IN}=12V with typical T_A=25°C, unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Voltage Operating Range	V_{IN}		8		40	V
V_{IN} UVLO Rising Threshold Voltage	V_{UVLO}	Input Voltage Rising			7	V
V_{IN} UVLO Hysteresis	V_{UVLO_YHS}	Input Voltage Falling		1		V
Standby Current	I_{SB}	V_{IN}=12V, V_{OUT}=5V, No Load		3		mA
Feedback Voltage	V_{FB}			0.8		V
Feedback Voltage Accuracy	ΔV_{FB}		-1.5		+1.5	%
Internal Soft Start Time	T_{SS}			10		mS
Hith Site Switch ON-Resistance	$R_{DS(ON)\_HI}$			120		mΩ
Max. Duty Cycle	D_{MAX}			85		%
Switching Frequency	f_{OSC}	V_{FB}=0.8V	175	200	225	KHz
Constant Current	I_{CC}	AME5242-AZAADJ-10		1.6		A
		AME5242-AZAADJ-24		2.7		A
Thermal Shutdown	T_{SD}			150		°C
Thermal Shutdown Hysteresis	ΔT_{SD}			20		°C
D+ D- Short Resistance	R_{D_short}	CTL x configured for DCP BC1.2		80	200	Ω
D- Output Voltage	V_{D-_AM}	CTLx configured for divider mode	1.9	2	2.4	V
D+ Output Voltage	V_{D+_AM}		2.57	2.7	2.84	V
D- Output Impedance	Z_{OUT_D-}		24	32	40	KΩ
D+ Output Impedance	Z_{OUT_D+}		24	32	40	KΩ
Output OVP	$V_{OV\text{-}OUT}$		V_{OUT} x 1.06		V_{OUT} x 1.16	V
Input OVP	$V_{OV\text{-}IN}$		32	35	40	V
Input OVP Hysteresis				2		V
Short Current Limit				2		A

■ Detailed Description

Under Voltage Lockout (UVLO)

The AME5242 incorporates an under voltage lockout circuit to keep the device disabled when V_{IN} (the input voltage) is below the UVLO rising threshold voltage. Once the UVLO rising threshold voltage is reached,the device start-up begins. The device operates until V_{IN} falls below the UVLO falling threshold voltage. The typical hysteresis in the UVLO comparator is 1V.

Over Voltage Protection

The AME5242 has input and output over-voltage protections. The thresholds of input and output OVP circuit include are typicapl 35V and minimum 106% x V_{OUT}, respectively. Once the input voltage or output voltage is higher than the threshold, the high-side MOSFET is turned off. When the input voltage or output voltage drops lower than the threshold, the high-side MOSFET will be enabled again.

Over Current Protection

The AME5242 cycle-by-cycle limits the peak inductor current to protect embedded switch from dameage. High-side switch current limiting is implemented by monitoring the current through the high side MOSFET.

Thermal Shutdown

The AME5242 protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown trip point, the high-side MOSFET is turned off. The part is restarted when the junction temperature drops 20°C below the thermal shutdown trip point

Setting the Output Voltage

The output voltage is using a resistive voltage divider connected from the output voltage to FB. It divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{out} \times \frac{R_2}{R_1 + R_2}$$

the output voltage is:

$$V_{out} = 0.8 \times \frac{R_1 + R_2}{R_2}$$

Inductor Selection

The inductor is required to supply contant current to the load while being driven by the switched input voltage. A larger value inductor will have a larger physical size and higher series resistance. It will result in less ripple current that will in turn result in lower output ripple voltage. Make sure that the peak inductor current is below the maximum switch current limit. Determine inductance is to allow the peak-to-peak ripple current to be approximately 30% of the maximum load current. The inductance value can be calculated by:

$$L = \frac{V_{out}}{f_s \times \Delta I_L} \times \left(1 - \frac{V_{out}}{V_{in}}\right)$$

Where f_S is the switching frequency, V_{IN} is the input voltage, V_{OUT} is the output voltage, and ΔI_L is the peak-to-peak inductor ripple current. Choose an inductor that will not saturate under the maximum inductor peak current, calculated by:

$$I_{LPK} = I_{LOAD} + \frac{V_{out}}{2 \times f_s \times L} \times \left(1 - \frac{V_{out}}{V_{in}}\right)$$

Where I_{LOAD} is the load current. The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI constraints.

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors will also be suggested. Choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current tating. The RMS current in the input capacitor can be esimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{out}}{V_{in}} \times \left(1 - \frac{V_{out}}{V_{in}}\right)}$$

At V_{IN}=2V_{OUT}, where I_{C1} = I_{LOAD}/2 is the worst-case condition occurs. For simplification, use an input capacitor with a RMS current rating greater than half of the maximum load current. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. When using electrolytic or tantalum capacitors, a high quality, small ceramic capacitor, i.e. 0.1µF, should be placed as close to the IC as possible. The input voltage ripple for low ESR capacitors can be estimated by:

$$I_{C1} = \frac{I_{LOAD}}{C1 \times f_s} \times \frac{V_{out}}{V_{in}} \times \left(1 - \frac{V_{out}}{V_{in}}\right)$$

Where C1 is the input capacitance value.

Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolutic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{out} = \frac{V_{out}}{f_s \times L} \times \left(1 - \frac{V_{out}}{V_{in}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C2}\right)$$

Where R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor and C2 is the output capacitance value.

When using ceramic capacitors, the impandance at the switching frequency is dominated by the capacitance which is the main cause for the output voltage ripple. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{out} = \frac{V_{out}}{8 \times f_s^2 \times L \times C2} \times \left(1 - \frac{V_{out}}{V_{in}}\right)$$

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{out} = \frac{V_{out}}{f_s \times L} \times \left(1 - \frac{V_{out}}{V_{in}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system.

Rectifier Diode

Use a Schottky diode as the rectifier to conduct current when the High-Side MOSFET is turned off. The Schottky diode must have current rating higher than the maximum output current and a reverse voltage rating higher than the maximum input voltage.

Compensation Components

AME5242 has current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero combination to govern the characteristics of the control system. The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{EA} \times \frac{V_{FB}}{V_{out}}$$

Where V_{FB} is the feedback voltage (0.8V), A_{VEA} is the error amplifier voltage gain, G_{CS} is the current sense transconducductance and R_{LOAD} is the load resistor value. The system has two poles of importance. One is due to the output capacitor and the load resistor, and the other is due to the compansation capacitor (C4) and the output resistor of the error amplifier. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2 \times \pi \times C4 \times A_{VEA}}$$

$$f_{P2} = \frac{1}{2 \times \pi \times C2 \times R_{LOAD}}$$

Where G_{EA} is the error amplifier transconducductance. The system has one zero of importance, due to the compensation capacitor (C4) and the compensation resistor (R3). This zero is located at:

$$f_{Z1} = \frac{1}{2\times\pi\times C4\times R3}$$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$f_{ESR} = \frac{1}{2\times\pi\times C2\times R_{ESR}}$$

In this case, a third pole set by the second compensation capacitor (C5) and the compensation resistor (R3) is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$$f_{P3} = \frac{1}{2\times\pi\times C5\times R3}$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system instability. A good standard is to set the crossover frequency below one-tenth of the switching frequency. To optimize the compensation components, the following procedure can be used.

1. Choose the compensation resistor (R3) to set the desired crossover frequency.

Determine R3 by the following equation:

$$R3 = \frac{2\times C2\times f_c}{G_{EA}\times G_{CS}}\times\frac{V_{out}}{V_{FB}} < \frac{2\times C2\times 0.1\times f_c}{G_{EA}\times G_{CS}}\times\frac{V_{out}}{V_{FB}}$$

Where f_C is the desired crossover frequency which is typically below one tenth of the switching frequency.

2. Choose the compensation capacitor (C4) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero (f_{Z1}) below one-forth of the crossover frequency provides sufficient phase margin.

Determine C4 by the floolwing equation:

$$C4 > \frac{4}{2\times\pi\times R3\times f_c}$$

Where R3 is the compensation resistor.

3. Determine if the second compensation capacitor (C5) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency, or the following relationship is valid:

$$\frac{1}{2\times\pi\times C2\times R_{ESR}} < \frac{f_s}{2}$$

If this is the case, then add the second compensation capacitor (C5) to set the pole f_{P3} at the location of the ESR zero. Determine C5 by the equation:

$$C5 = \frac{C2\times R_{ESR}}{R3}$$

PC Board Layout Guidance

When laying out the printed circuit board, the following checklist should be uesd to ensure proper operation of the IC.

1) Arrange the power components to reduce the AC loop size consisting of C_{IN}, IN pin, SW pin and the sckottky diode.

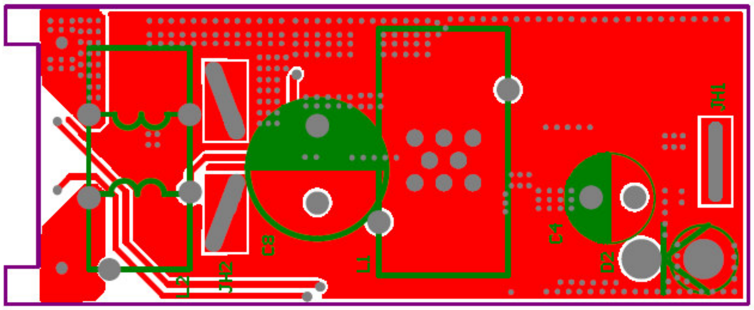
2) Place input decoupling ceramic capacitor C_{IN} as close to IN pin as possible. C_{IN} is connected power GND with vias or short and wide path.

3) Return FB and COMP to signal GND pin, and connect the singal GND to power GND at a single point for the best noise immunity. Connect exposed pad to power ground copper area with copper and vias.

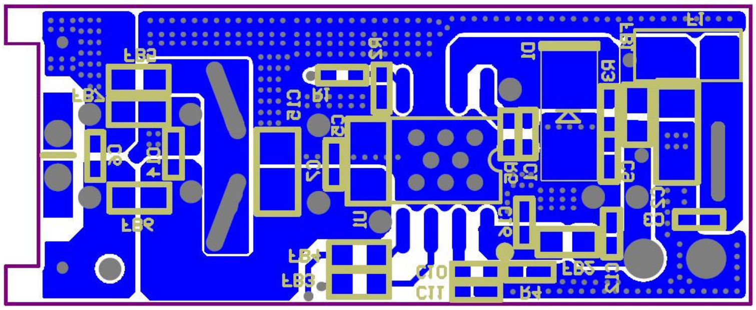
4) Use copper plane for power GND for best heat disspation and noise immunity.

5) Please feedback resistor close to FB pin.

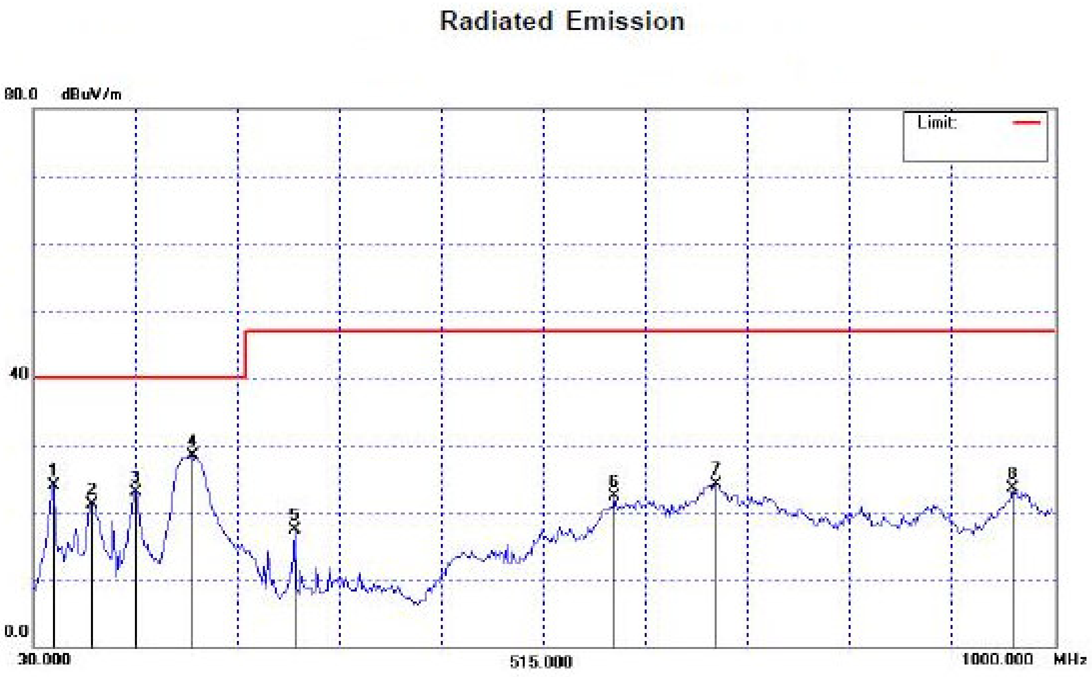
Top Layer



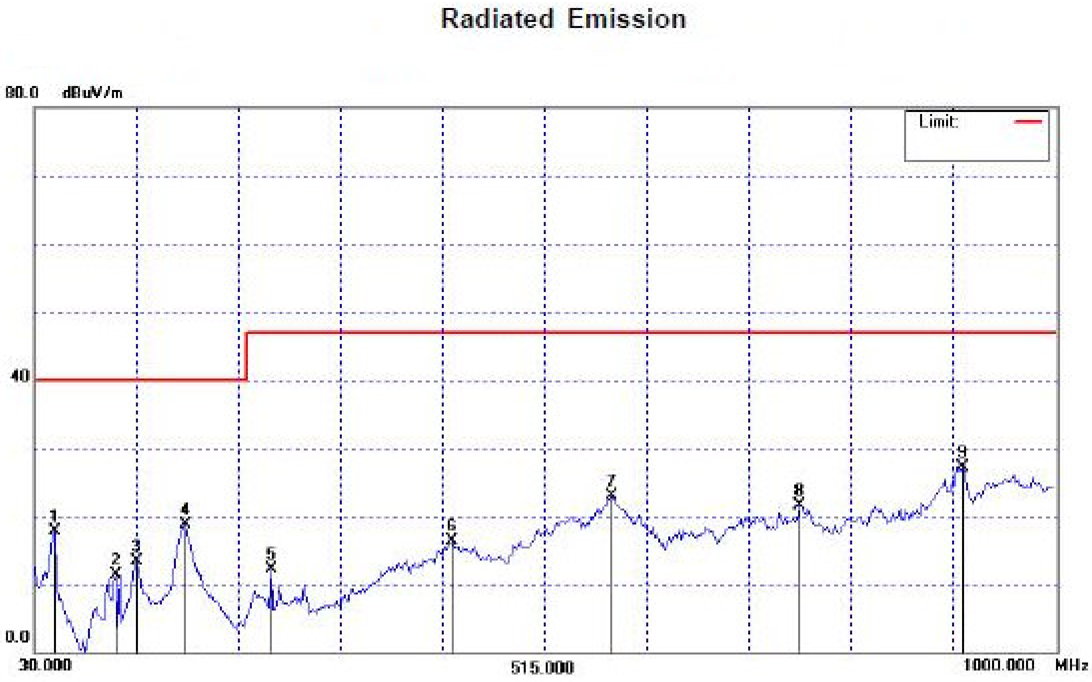
Bottom Layer



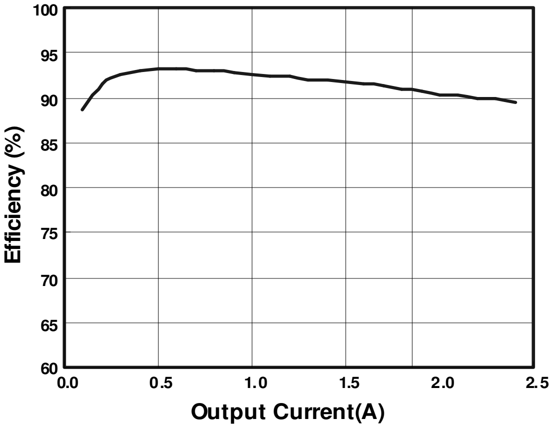
■ Radiated EMI Data (Vertical)

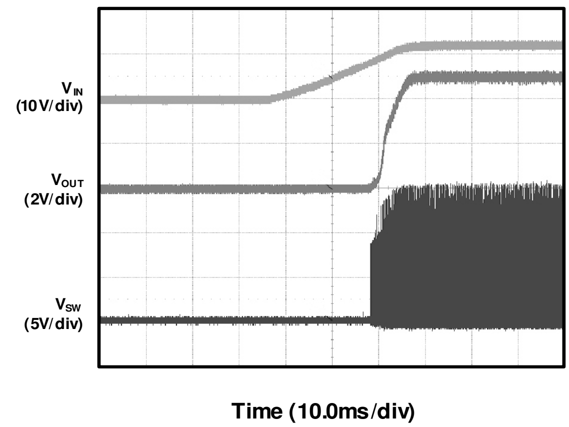


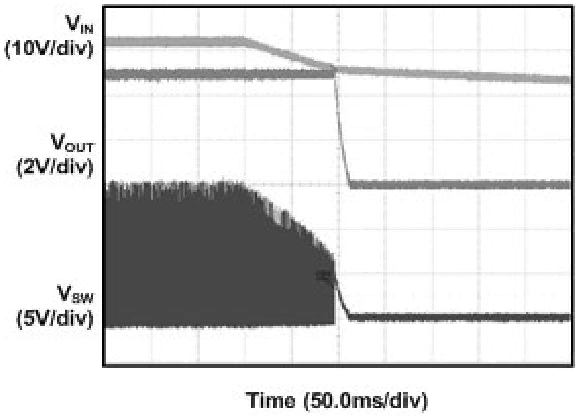
■ Radiated EMI Data (Horizontal)

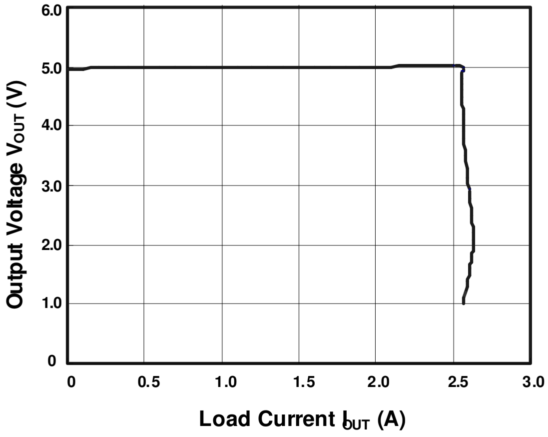


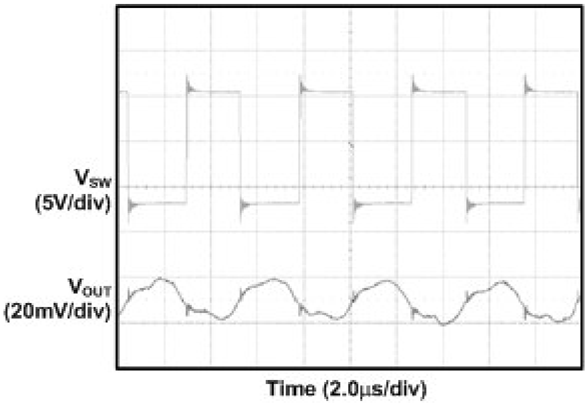
■ Characterization Curve

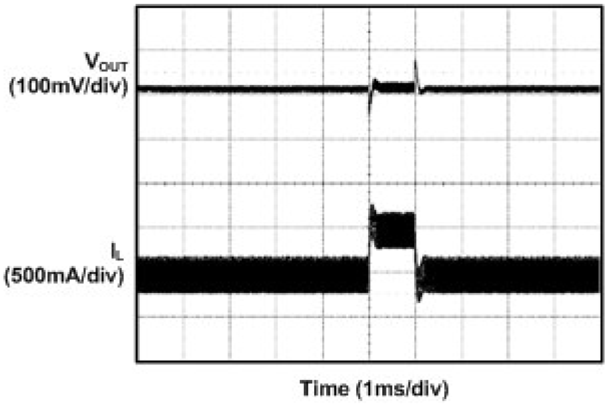

Efficiency vs. Output Current


Power ON from V_{IN}


Power Off from V_{IN}

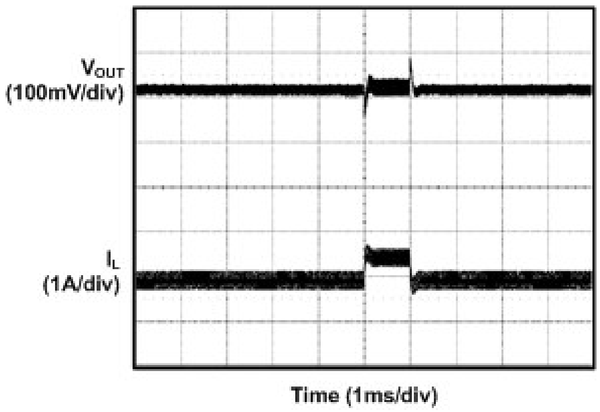

I-V Curve


Full Load Ripple

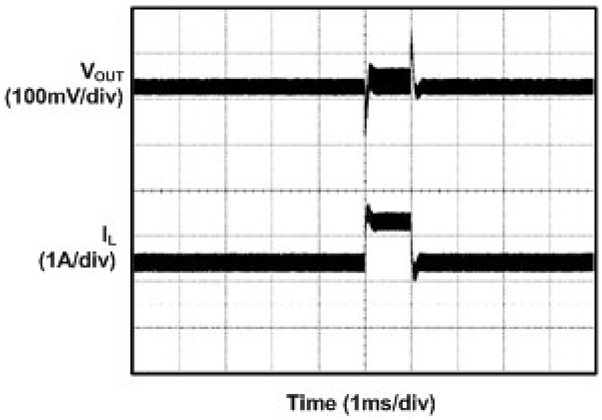

Load Transient Response

■ Characterization Curve

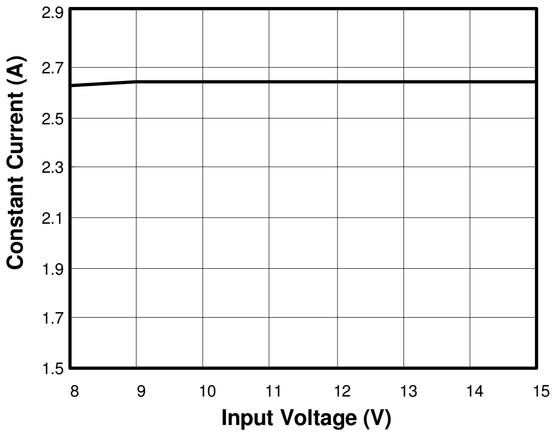
Load Transient Response



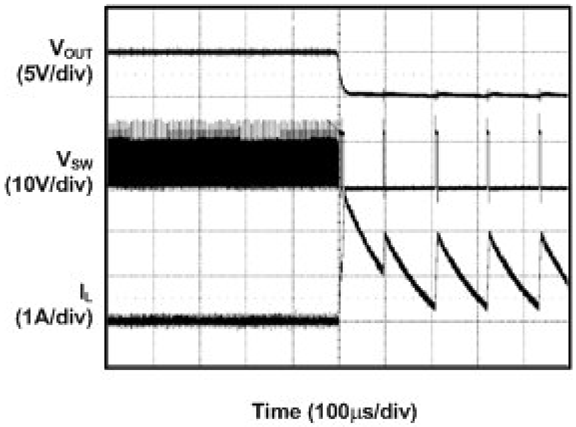
Load Transient Response



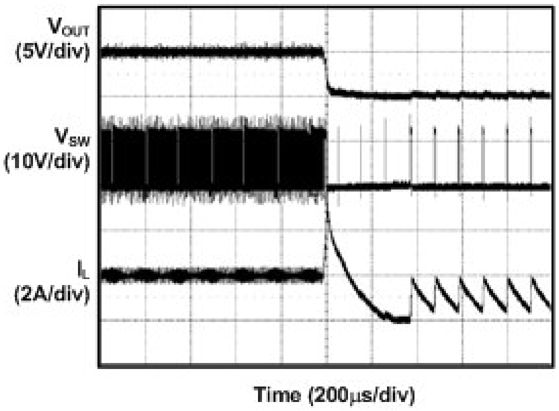
Input Voltage vs. Constant Current



0A Short

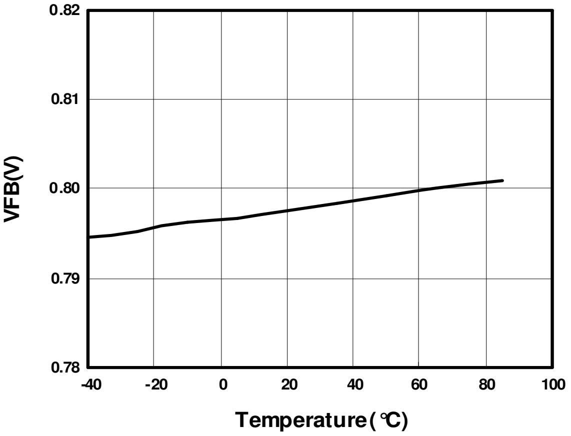


2A Short

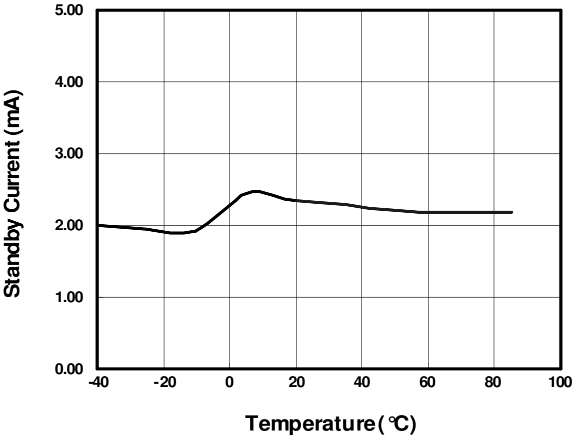


■ Characterization Curve

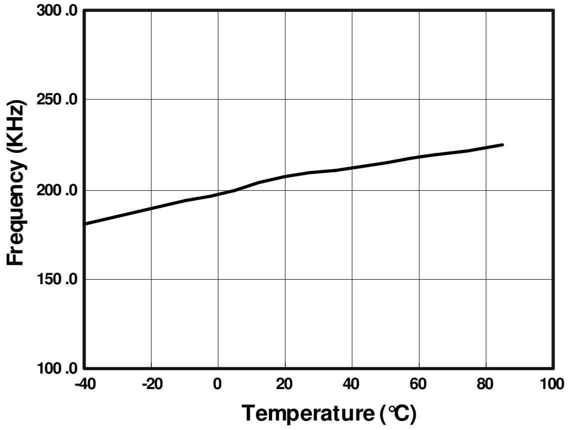
V_{FB} vs. Temperature



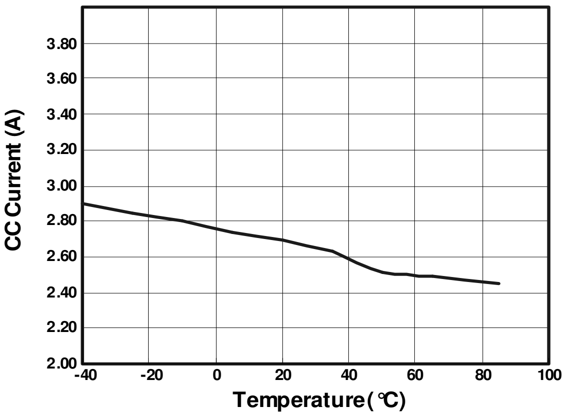
Stanby Current vs. Temperature



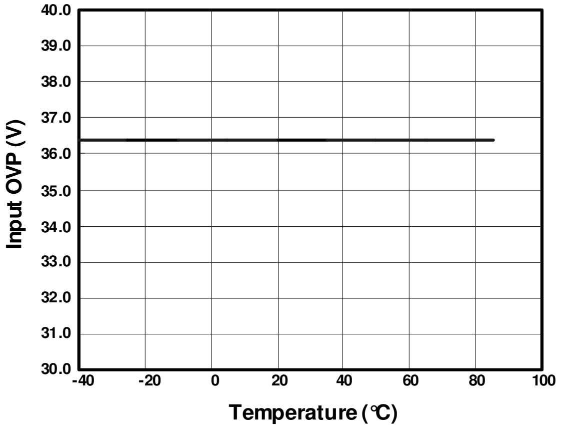
Frequency vs. Temperature



CC Current vs. Temperature

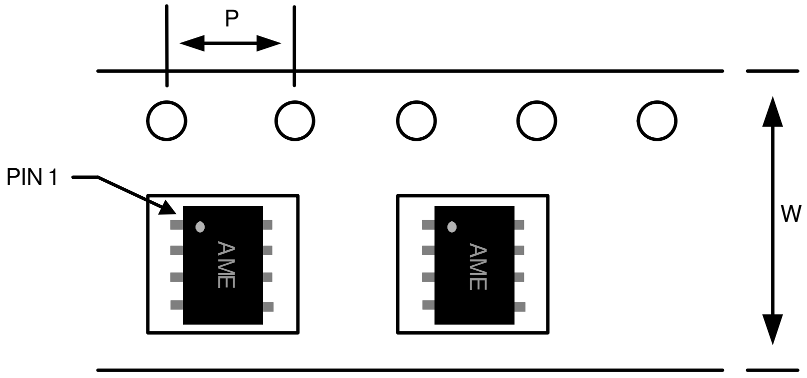


Input OVP vs. Temperature



■ Tape and Reel Dimension

SOP-8/PP

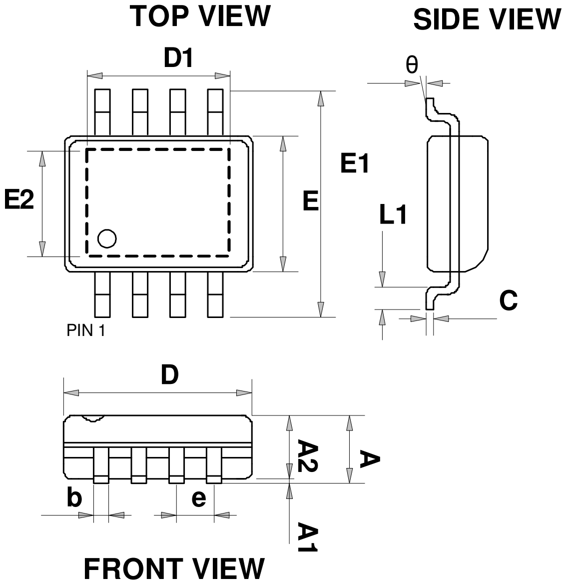


Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
SOP-8/PP	12.0±0.1 mm	4.0±0.1 mm	2500pcs	330±1 mm

■ Package Dimension

SOP-8/PP


TOP VIEW

SIDE VIEW

FRONT VIEW

SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.000	0.250	0.000	0.010
A2	1.250	1.650	0.049	0.065
C	0.100	0.250	0.004	0.010
E	3.750	4.150	0.148	0.163
E1	5.700	6.300	0.224	0.248
L1	0.300	1.270	0.012	0.050
b	0.310	0.510	0.012	0.020
D	4.720	5.120	0.186	0.202
e	1.270 BSC		0.050 BSC	
θ	0°	8°	0°	8°
E2	1.940	2.600	0.076	0.102
D1	1.940	3.500	0.076	0.138

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