5.5V, 6A, 23mΩ Single Channel Load Switch

■ General Description

The AME6204 is a small, low R_{ON}, single-channel load switch with enable function. The device contains a N-channel MOSFETs that can operate over an input voltage range of 0.8V to 5.5V and can offer a maximum continuous current of 6A.

The EN pin is controlled by an on and off input, which can be driven directly by low-voltage control signals. In AME6204, a 225Ω on-chip load resistor is added for quick-output discharge when AME6204 is turned off. It's available in a small, space-saving DFN-8D (2 x 2 x 0.75mm) package with thermal pad allowing for high power dissipation.

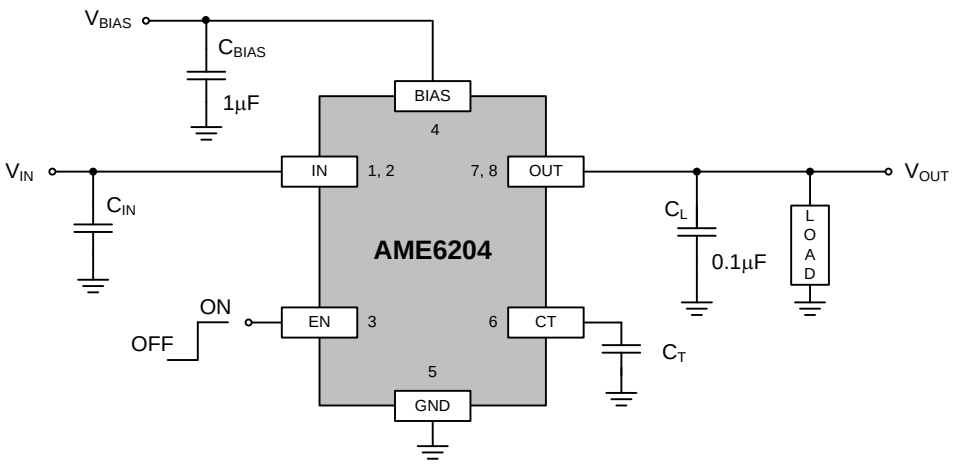
■ Features

- Input Voltage Range: 0.8V to 5.5V
- Bias Voltage Supports: 2.5V to 5.5V
- Integrated Single-Channel Load Switch
- 6A Maximum Continuous Current
- Ultra low $R_{DS(ON)}$ 23mΩ
- Low Quiescent Current (46μA)
- Thermal Protection
- Adjustable Rise Time
- Quick Output Discharge (QOD)
- DFN-8D (2 x 2 x 0.75mm) Package with Thermal Pad
- RoHS Compliant

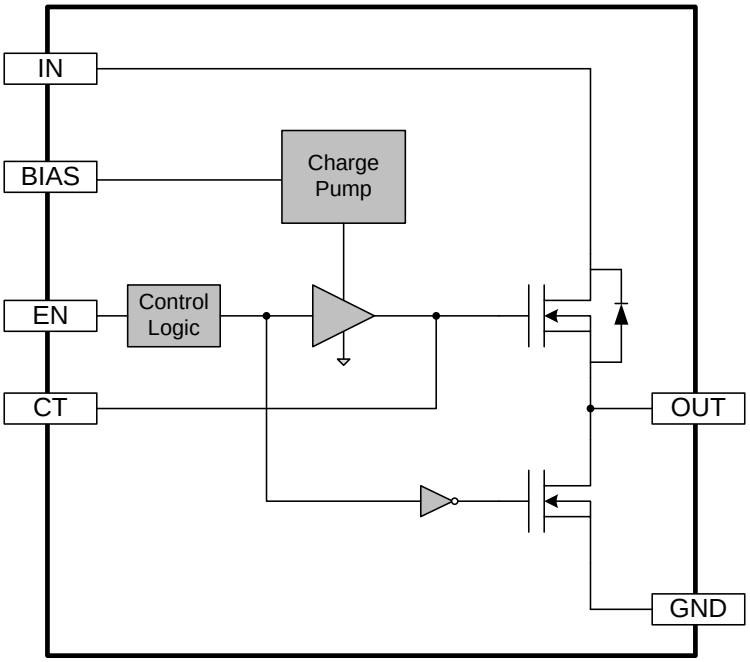
■ Application

- Ultrabook, Notebooks and Netbooks
- Tablet PCs
- Consumer Electronics
- Set-top Boxes and Residential Gateways
- Telecom Systems
- Solid-State Drives (SSD)

■ Typical Application Schematic

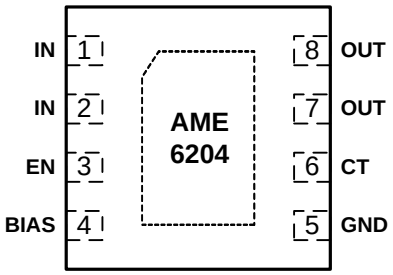


■ Function Block Diagram



■ Pin Configuration

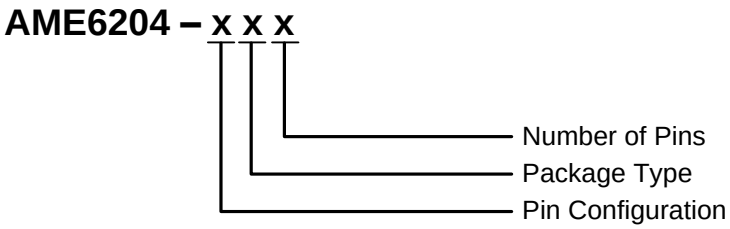
Top View
DFN-8D (2x2x0.75mm)



■ Pin Description

Pin Name	Pin No.	I/O	Description
IN	1, 2	I	Power-switch input. 0.8V to BIAS voltage range for optimal $R_{DS(ON)}$ is recommended. Place an optional decoupling capacitor between this pin and GND for reduce input voltage dip during turn on.
EN	3	I	ON/OFF control input. Active high is turn-on. Do not leave it floating.
BIAS	4	I	Bias voltage input. Recommend voltage range (2.5V to 5.5V) to supply the device.
GND	5	-	Ground
CT	6	I	Power-switch slew-rate control. Capacitor must be rated for a minimum of 25V for desired rise time performance. This pin can be left floating.
OUT	7, 8	O	Power-switch output.

■ Ordering Information



Pin Configuration	Package Type	Number of Pins
A: 1. IN 2. IN 3. EN 4. BIAS 5. GND 6. CT 7. OUT 8. OUT	V: DFN	A: 8

■ Absolute Maximum Ratings

Parameter		Value	Unit
Input Voltage		-0.3 to +6	V
BIAS Voltage (BIAS)		-0.3 to +6	V
Output Voltage		-0.3 to +6	V
Enable Voltage		-0.3 to +6	V
Output Current (Continuous)		6	A
Output Current (Pulsed) (Note1)		8	A
ESD Ratings	HBM	±2000	V
	MM	±400	V
	CDM	±1000	V

Note1: Maximum pulsed current switch , pulse < 300μs, 3% duty cycle.

■ Recommended Operation Conditions

Parameter	Symbol	Value	Unit
Input Voltage	V_{IN}	0.8 to V_{BIAS}	V
BIAS Voltage	V_{BIAS}	2.5 to 5.5	V
Enable Voltage	V_{EN}	0 to 5.5	V
Ambient Temperature Range	T_A	-40 to +85	°C
Junction Temperature Range	T_J	-40 to +125	
Storage Temperature	T_{STG}	-65 to +150	

■ Thermal Information

Parameter	Package	Die Attach	Symbol	Maximum	Unit
Thermal Resistance* (Junction to Case)	DFN-8D	Conductive Epoxy	θ_{JC}	16	°C / W
Thermal Resistance (Junction to Ambient)	DFN-8D	Conductive Epoxy	θ_{JA}	66	°C / W
Internal Power Dissipation	DFN-8D	Conductive Epoxy	P_D	1515	mW
Lead Temperature (soldering 10 sec)**				300	°C

* Measure θ_{JC} on backside center of Exposed Pad.

** MIL-STD-202G210F

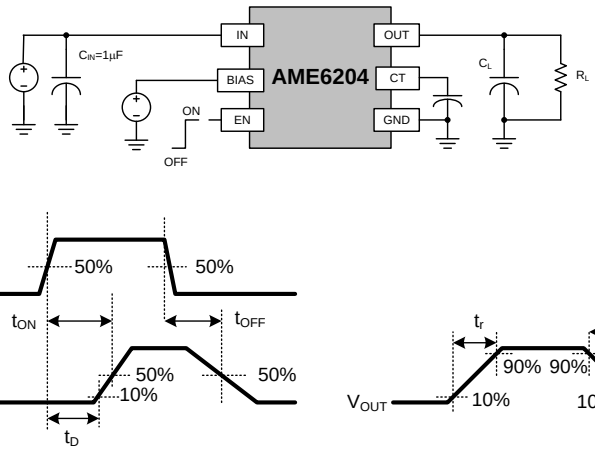
■ Electrical Specifications

V_{BAIS} = 5V, V_{IN} = 5V, T_J = 25°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
BIAS Pin Quiescent Current	I_Q	I_{OUT} = 0mA, V_{BIAS} = 5V, V_{EN} = 5V		46	72	μA
		I_{OUT} = 0mA, V_{BIAS} = 2.5V, V_{EN} = 2.5V		28	37	μA
BIAS Pin Shutdown Current	I_{SHDN_BIAS}	V_{EN} = 0V		0.1	1	μA
IN Pin Shutdown Current	I_{SHDN_IN}	V_{EN} = 0V, V_{IN} = 0.8V to 5V		0.1	1	μA
EN Pin Current	I_{EN}	V_{EN} = 5.5V		0.1	1	μA
ON Resistance	$R_{DS(ON)}$	I_{OUT} = 200mA, V_{BIAS} = 5V, V_{IN} = 0.8V to 5V		23	30	mΩ
		I_{OUT} = 200mA, V_{BIAS} = 2.5V, V_{IN} = 0.8V to 2.5V		24	31	mΩ
Output Discharge Resistance	R_{DSG}	V_{IN} = V_{BIAS} = 5V		225	300	Ω
		V_{IN} = V_{BIAS} = 2.5V		275	325	Ω
EN Pin High Level	V_{EN_H}		1.2			V
EN Pin Low Level	V_{EN_L}				0.6	V
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{SDHY}			30		°C

■ Parameter Measurement Information

Single Channel Shown



Parameter	Symbol	Test Condition	Min	Typ	Max	Units
V_{IN} = 5V, V_{EN} = V_{BIAS} = 5V, T_A = 25°C						
Turn-on Time	T_{ON}	R_L = 10Ω, C_L = 0.1μF, C_T = 1nF		1320		μS
Turn-off Time	T_{OFF}	R_L = 10Ω, C_L = 0.1μF, C_T = 1nF		2		μS
V_{OUT} Rise Time	T_R	R_L = 10Ω, C_L = 0.1μF, C_T = 1nF		1768		μS
V_{OUT} Fall Time	T_F	R_L = 10Ω, C_L = 0.1μF, C_T = 1nF		3		μS
ON Delay Time	T_D	R_L = 10Ω, C_L = 0.1μF, C_T = 1nF		272		μS
V_{IN} = 0.8V, V_{EN} = V_{BIAS} = 5V, T_A = 25°C						
Turn-on Time	T_{ON}	R_L = 10Ω, C_L = 0.1μF, C_T = 1nF		340		μS
Turn-off Time	T_{OFF}	R_L = 10Ω, C_L = 0.1μF, C_T = 1nF		20		μS
V_{OUT} Rise Time	T_R	R_L = 10Ω, C_L = 0.1μF, C_T = 1nF		225		μS
V_{OUT} Fall Time	T_F	R_L = 10Ω, C_L = 0.1μF, C_T = 1nF		3		μS
ON Delay Time	T_D	R_L = 10Ω, C_L = 0.1μF, C_T = 1nF		220		μS
V_{IN} = 2.5V, V_{EN} = V_{BIAS} = 2.5V, T_A = 25°C						
Turn-on Time	T_{ON}	R_L = 10Ω, C_L = 0.1μF, C_T = 1nF		2900		μS
Turn-off Time	T_{OFF}	R_L = 10Ω, C_L = 0.1μF, C_T = 1nF		2		μS
V_{OUT} Rise Time	T_R	R_L = 10Ω, C_L = 0.1μF, C_T = 1nF		2800		μS
V_{OUT} Fall Time	T_F	R_L = 10Ω, C_L = 0.1μF, C_T = 1nF		3		μS
ON Delay Time	T_D	R_L = 10Ω, C_L = 0.1μF, C_T = 1nF		1260		μS
V_{IN} = 0.8V, V_{EN} = V_{BIAS} = 2.5V, T_A = 25°C						
Turn-on Time	T_{ON}	R_L = 10Ω, C_L = 0.1μF, C_T = 1nF		1890		μS
Turn-off Time	T_{OFF}	R_L = 10Ω, C_L = 0.1μF, C_T = 1nF		10		μS
V_{OUT} Rise Time	T_R	R_L = 10Ω, C_L = 0.1μF, C_T = 1nF		1100		μS
V_{OUT} Fall Time	T_F	R_L = 10Ω, C_L = 0.1μF, C_T = 1nF		3		μS
ON Delay Time	T_D	R_L = 10Ω, C_L = 0.1μF, C_T = 1nF		1140		μS

■ Application Information

Input Capacitor (Optional)

Place a 1μF ceramic capacitor, C_{IN} between IN and GND as close as possible to the pins to limit the voltage drop on the input supply caused by inrush current when the power switch turns on into a discharged load capacitor. Recommend to adopt an input capacitance about 10 times higher than output one to prevent from excessive voltage drop when switching heavy load.

Output Capacitor (Optional)

Because of the body diode in NMOS, it is recommended to use a C_{IN} greater than C_L. If a C_L is greater than C_{IN}, it will cause V_{OUT} to exceed V_{IN} while the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}.

A C_{IN} : C_L = 10:1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup, however a 10:1 ratio for capacitance is not required for proper functionality of the device. If a ratio is smaller than 10 (such as 1), it will cause slightly more V_{IN} dip upon turn on due to inrush currents. This can be mitigated by increasing the capacitance on the C_T pin for a longer rise time (see the **Adjustable Rise Time** section).

ON and OFF Control

The EN pins control the state of AME6204. Asserting EN pin high activates the switch. EN pin is active-high with a low threshold, making it capable of interfacing with low-voltage signals. The EN pin can be applied by standard GPIO logic threshold. It can be used with any microcontroller with 1.2V or higher GPIO voltage. Do not make the pin floating and must be tied either high or low for proper functionality.

Quick Output Discharge (QOD)

When AME6204 is disabled, an internal discharge resistance is automatically connected between OUT and GND, thus discharge the remaining charge from the output. This resistance prevents the output from floating while the switch is disabled. For best results, it is recommended that AME6204 gets disabled before V_{BIAS} falls below the minimum recommended voltage.

Device Functional Modes

EN	IN to OUT	OUT to GND
H	ON	OFF
L	OFF	ON

Power Dissipation

The maximum IC junction temperature must be restricted to 125°C under normal operating conditions. To calculate the maximum allowable power dissipation

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}}$$

where

- $P_{D(max)}$ is the maximum allowable power dissipation.
- $T_{J(max)}$ is the maximum allowable junction temperature.
- T_A is the ambient temperature of the device.
- θ_{JA} is the junction to air thermal impedance. This parameter is highly dependent upon board layout.

■ Application Information (Contd.)

V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device will still be functional if $V_{IN} > V_{BIAS}$ but it will exhibit R_{ON} greater than what is shown in the **Characterization Curve "V_{IN} v.s R_{ON}"**.

Adjustable Rise Time

Place a capacitor between CT pin and GND to set the rise time of OUT pin. To ensure desired performance, a capacitor with a minimum voltage rating of 25 V must be applied on either CT pins. An approximate formula for the relationship between CT and rise time is (Equation accounts for 10% to 90% measurement on V_{OUT}):

Rise Time (μS) = (C_T + 39) * V_{OUT} * 0.36 + 21

where C_T is the capacitance value on the CT pin (in pF)

Rise time values measured on a typical device is shown as Table 1. Rise times shown below are only valid for the power-up sequence where IN and BIAS are already in steady state condition, and the EN pin is asserted high.

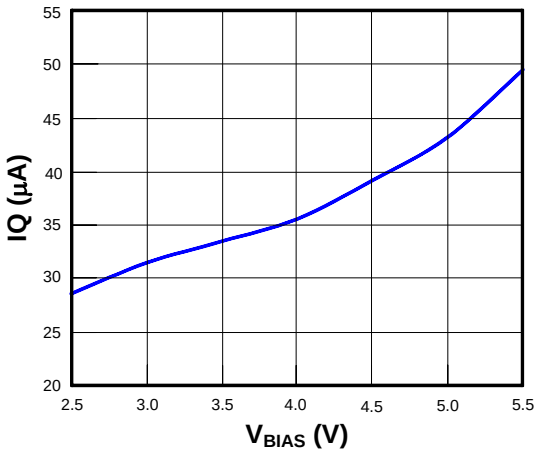
Table 1. Rise Times on a typical device

C_T (pF)	Rise Time (μs) 10% ~ 90%, C_L= 0.1μF, C_{IN} = 1μF, R_L = 10Ω(1)						
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	0.8V
0	90.46	69.41	49.06	45.01	41.05	38.62	34.1
220	462.7	277.6	118.7	88.06	57.82	41.36	30
470	925.3	579.2	272.1	204.3	141.8	113.4	54.9
1000	1759	1122	557.7	437.4	313	260.3	150.1
2200	3965	2467	1285	1052	768.2	670.1	440.6
4700	8199	5240	2814	2266	1742	1450	1012
10000	20210	12090	6443	5391	4245	3639	2511

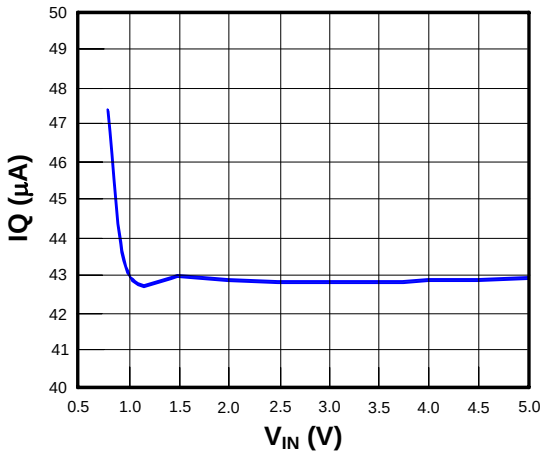
(1) Typical Values at 25°C, V_{BIAS} = 5V, 15V X7R 10% Ceramic Capacitor

■ Characterization Curve

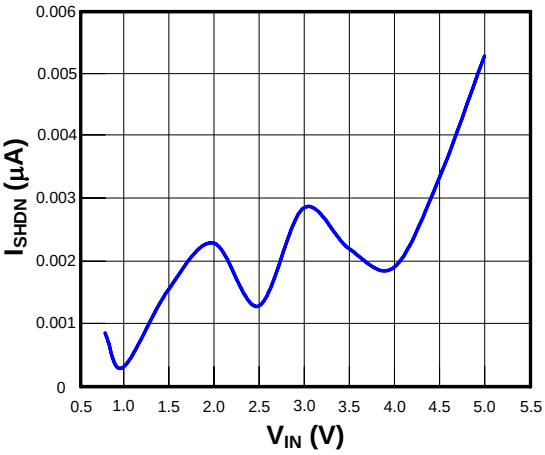
I_Q with V_{BIAS}



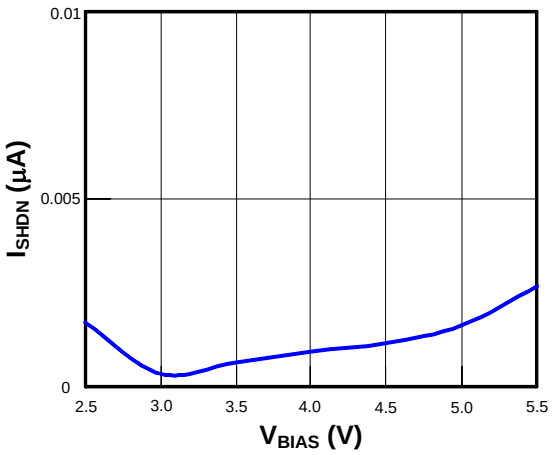
I_Q with V_{IN}



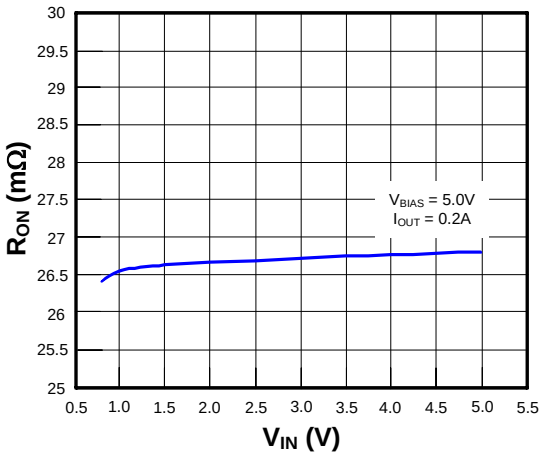
I_{SHDN} v.s V_{IN}



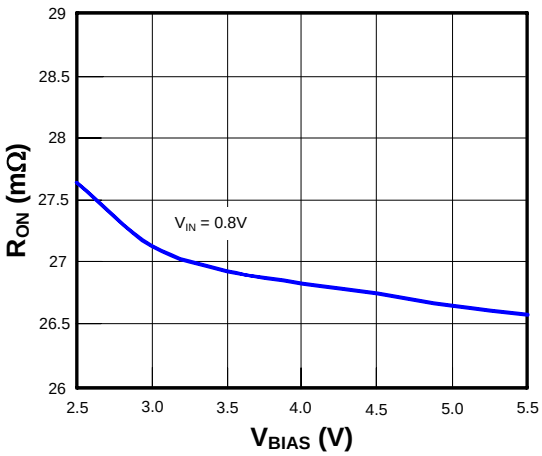
I_{SHDN} v.s V_{BIAS}



V_{IN} v.s R_{ON}



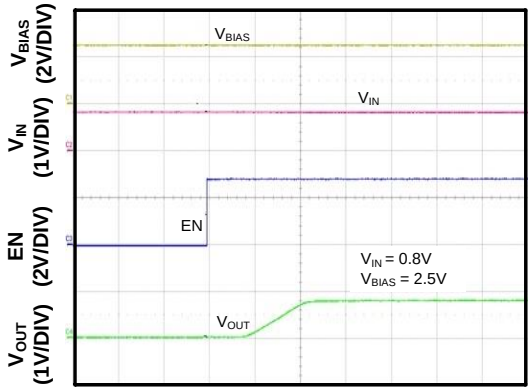
V_{BIAS} v.s R_{ON}



■ Characterization Curve (Contd.)

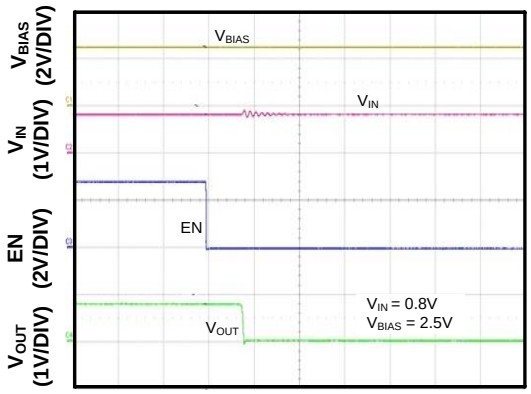
C_{IN} = 1μF, C_{OUT} = 0.1 μF, R_L = 10Ω, C_T = 1nF

Turn ON Response Time



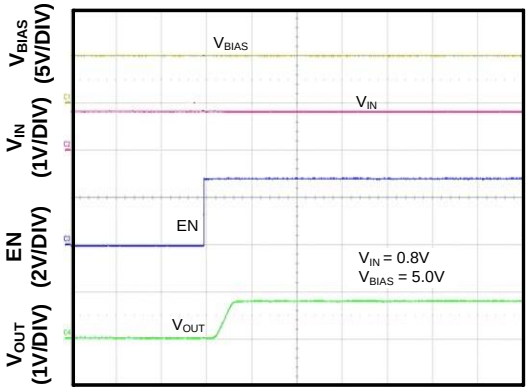
Time (1ms/DIV)

Turn OFF Response Time



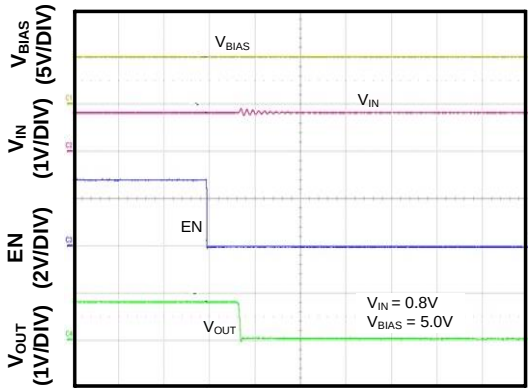
Time (50μs/DIV)

Turn ON Response Time



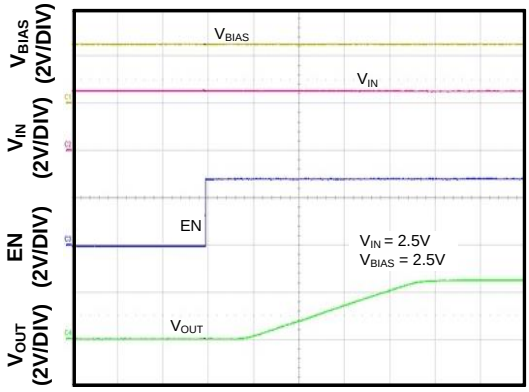
Time (1ms/DIV)

Turn OFF Response Time



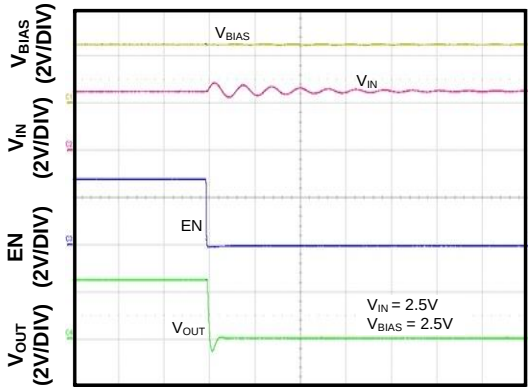
Time (50μs/DIV)

Turn ON Response Time



Time (1ms/DIV)

Turn OFF Response Time

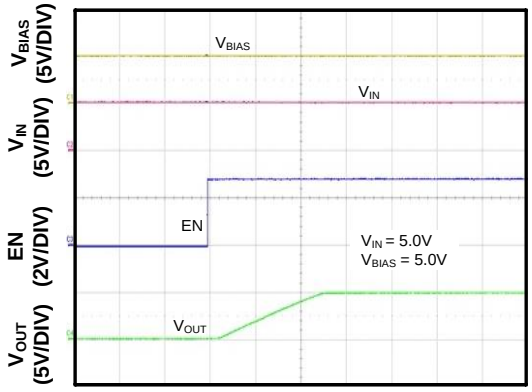


Time (10μs/DIV)

■ Characterization Curve (Contd.)

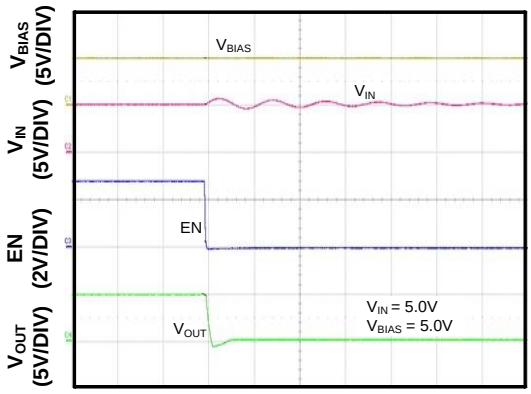
C_{IN} = 1μF, C_{OUT} = 0.1 μF, R_L = 10Ω, C_T = 1nF

Turn ON Response Time



Time (1ms/DIV)

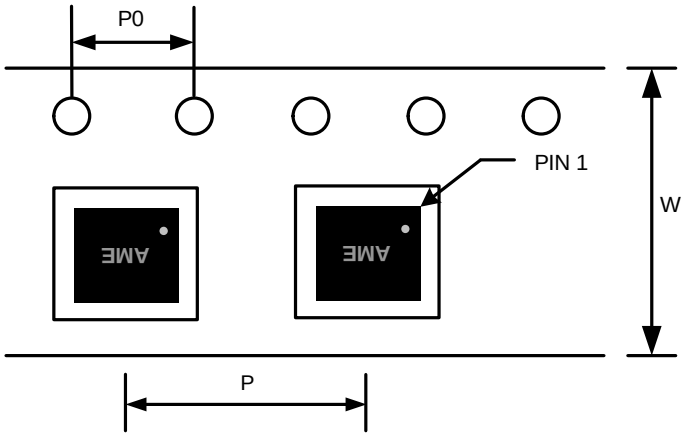
Turn OFF Response Time



Time (5μs/DIV)

■ Tape and Reel Dimension

DFN-8D
(2x2x0.75mm)

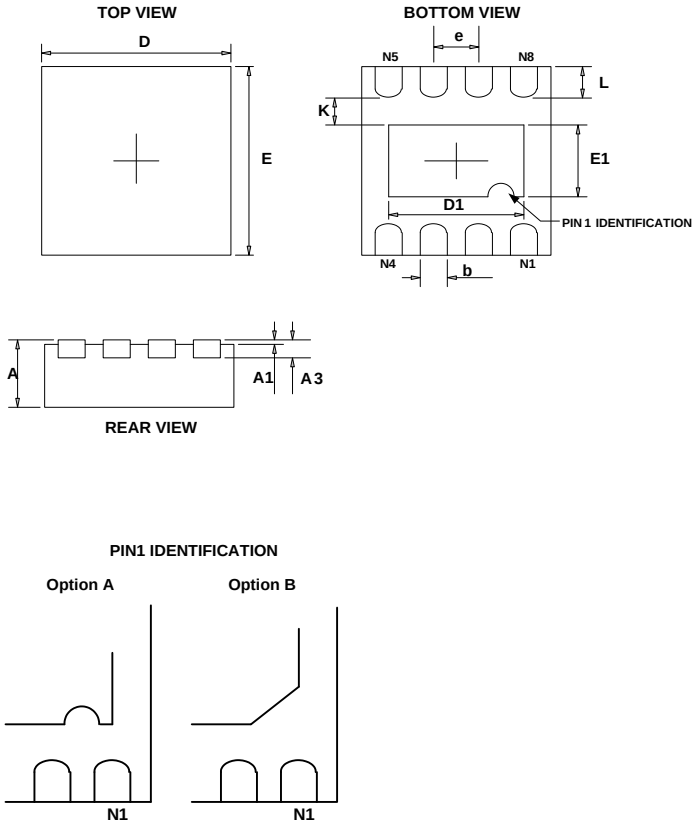


Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Pitch (P0)	Part Per Full Reel	Reel Size
DFN-8D	8.0±0.1 mm	4.0±0.1 mm	4.0±0.1 mm	3000pcs	180±1 mm

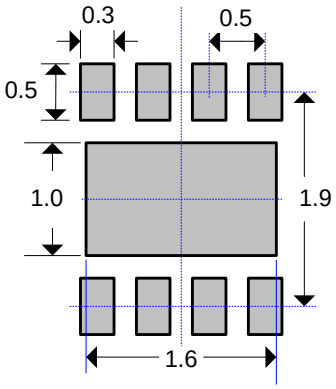
■ Package Dimension

DFN-8D
(2x2x0.75mm)



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203 REF		0.008 REF	
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
D1	1.100	1.650	0.043	0.065
E1	0.500	0.950	0.020	0.037
K	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.200	0.450	0.008	0.018

■ Lead Pattern



Note:

1. Dimensions in Millimeters.
2. General tolerance ±0.05mm unless otherwise specified.

www.ame.com.tw

E-mail: sales@ame.com.tw

Life Support Policy:

These products of AME, Inc. are not authorized for use as critical components in life-support devices or systems, without the express written approval of the president of AME, Inc.

AME, Inc. reserves the right to make changes in the circuitry and specifications of its devices and advises its customers to obtain the latest version of relevant information.

© AME, Inc. , March 2023

Document: P004-DS6204-D.02

Corporate Headquarter

AME, Inc.

8F-1, 12, WenHu St., Nei-Hu Dist.,

Taipei 114, Taiwan..

Tel: 886 2 2627-8687

Fax: 886 2 2659-2989